RELIABILITY CHALLENGES AND MODELING OF MODERN SOLDERED ASSEMBLIES

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ABSTRACT

Miniaturized electronic assemblies have emerged that bring about new reliability challenges and, in some cases, have revived the concerns of leadless ceramic carriers on organic substrates. Many chip scale packages are leadless, have a low coefficient of thermal expansion and a low stand-off height. Typical assemblies are very fine-pitch with micro-solder joints having small load bearing areas. The above attributes may be detrimental to long term solder joint integrity and suggest that reliability be looked at carefully, more so than with conventional surface mount assemblies. This paper presents package and assembly thermal stress / reliability models that can help tackle those problems and ensure that assembly reliability is built-in during the early stages of product design. The models have been implemented in a PC-based design-for-reliability tool that enables quick parametric studies on chip, package, board and assembly parameters.

INTRODUCTION

Solder joint reliability may be defined as the ability of solder joints to provide interconnect electrical continuity throughout the intended design life of an electronic assembly. Under thermal loading conditions, solder joints fail in a fatigue / wear-out mode. Fatigue is driven by cyclic strains and stresses imparted to the solder joints by mismatches in Coefficients of Thermal Expansion (CTE) between the interconnected parts. The goal of reliability studies is to ensure that wear-out failure rates do not exceed specified failure levels for a given application. Engineering models have been developed (e.g. [1, 2]) that enable upfront life predictions and capture the main effects of design parameters and material properties on assembly reliability.

Studies [3, 4] have shown that the silicon contents and the multilayer construction of Ball Grid Array (BGA) and other low profile packages have a significant impact on assembly reliability. Similar concerns hold for Chip Scale Packages (CSP) with an even higher silicon contents. This paper addresses some of the reliability issues of CSP assemblies and presents engineering mechanics models that quantify the impact of CSP parameters on assembly reliability. Geometry of the package / assembly construction and measurement of material properties are critical input to the CSP assembly models.

SOLDER JOINT LIFE PREDICTIONS

Solder interconnect reliability modeling has been the subject of intensive studies for over 25 years [5]. Trade-offs between different models are in terms of accuracy, applicability, validity, cost, availability, ease of use and skills required. Models can be categorized based on the computational resources needed to run them. Existing capabilities range from technology specific, hand-held calculator models [5, 6] to PC-based [2, 7, 8] engineering mechanics models, finite element analysis on workstations [1], and supercomputer research models [9, 10].

Solder Reliability Solutions (SRS) [2] is a PC-based model that was initially developed for conventional surface mount assemblies. The model accounts for plastic flow and creep of solder, and includes local CTE mismatch effects and failure statistics. The correlation of accelerated test data uses inelastic strain energy as a measure of cyclic damage (Figure 1). On the vertical axis, the joint characteristic life scaled for the solder crack area is the inverse of a two-dimensional crack propagation rate. The SRS model has been validated over a wide range of test conditions and for common families of components assembled with eutectic or near-eutectic Sn-Pb. The data is from 30 experiments and covers three orders of magnitude along the x- and y-axis.
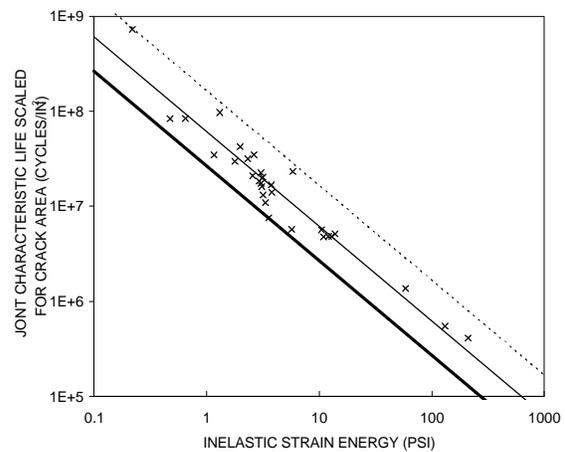

Figure 1: SRS correlation of test data (30 experiments).

Structural analysis in SRS uses simplified, one-dimensional engineering mechanics models for board/component interaction. The analysis, presented in details in [2], includes stretching and bending of parts for leadless assemblies, and lead stiffness parameters for leaded components. The following sections describe the structural analysis procedures that were developed to extend the model to two popular types of CSPs:

- Flip-chip with underfill
- Micro-BGA with compliant elastomer layer.

FLIP-CHIP WITH UNDERFILL

Assembly Model

The solder joint life improvement mechanism in flip-chip assemblies with underfill is easily conceptualized. Since the in-plane thermal expansion mismatch between die and substrate is taken up by shear of the solder joints *and* of the underfill layer, the solder joints see lesser strains than in bare chip assemblies. To a first order, the shear stiffness of the underfill layer determines the effectiveness of mechanical coupling between the die and substrate. Thus, a higher modulus underfill material provides for improved coupling and reduced shear strains on the solder joints. Engineering mechanics provide the tools to quantify those effects, as shown below and in appendix. The model that was developed for flip-chip with underfill [11] assumes that the CTE of the underfill material is close to that of solder (as is the case in most underfill assemblies) so the joints are not stretched in the out-of-plane direction.
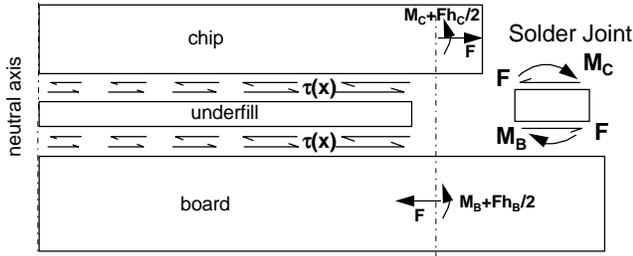
Figure 2: Interfacial shear stresses at die/underfill/substrate interfaces.

Figure 2 shows the assumed distribution of shear stresses, $\tau(x)$, at the underfill/die and underfill/substrate interfaces, as well as the shear forces (F) and bending moments (M's) exerted by solder joints on the die and substrate. The solution of the strength of materials problem depicted in Figure 2 is obtained by combining Hall's model of LCCC assemblies [12] and Suhir's theory of multilayer stacks and adhesive bonds [13] (see appendix). The interfacial shear stress distribution in the underfill layer follows a hyperbolic sine. The solder joint shear strain γ and shear force F obey the following stress reduction line equation:

$$h_U\gamma + \frac{F}{K_U} = \frac{1}{R}L\Delta\alpha\Delta T \qquad (1)$$

where h_U is the underfill or solder joint thickness, K_U is the assembly stiffness, L is the Distance to Neutral Point (DNP) of the outermost corner joint, $\Delta\alpha$ is the die to substrate CTE mismatch, ΔT is the temperature swing and R is a strain or CTE mismatch reduction factor. Equations for K_U and R are given in appendix. Both parameters depend on the thickness and material properties of each layer of the tri-layer stack, as well as assembly pitch and chip size. As shown in [11], when the modulus of the underfill material goes to zero, K_U converges to the assembly stiffness for an assembly without underfill and the strain reduction factor R goes to 1. K_U is *larger* than the assembly stiffness K for an assembly without underfill because mechanical coupling provided by the underfill layer stiffens the assembly. In general, this decrease in compliance is offset by a much larger reduction in the applied strain ($R \gg 1$ when the underfill modulus is high enough).

The assembly stiffness, K_U, the effective CTE mismatch $\Delta\alpha/R$ and the stress reduction line equation (2) are used to generate solder joint hysteresis loops. Figure 3 is a schematic of isothermal stress reduction lines in the force versus strain plane. For assemblies without underfill, the maximum applied strain is $\gamma_{max} = \dfrac{L\Delta\alpha\Delta T}{h_U}$, the maximum applied force is proportional to $K\Delta\alpha_G$, and the strain energy, or area of the triangle under the stress reduction line, goes as $K(\Delta\alpha_G)^2$. For the same assembly with underfill, the maximum effective strain that is seen by the solder joints is γ_{max}/R, the maximum shear force goes as $K_U\Delta\alpha/R$ (which is less than $K\Delta\alpha$, in general), and the strain energy goes as $K_U(\Delta\alpha/R)^2$. Using a strain energy criterion for solder fatigue, the mechanics of solder joints suggest a potentially significant improvement in fatigue life for assemblies with underfill compared to assemblies without underfill.
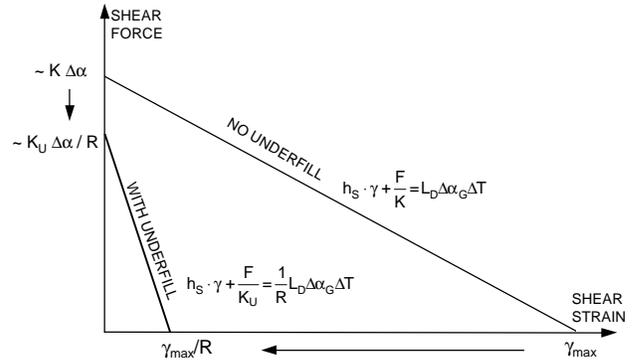

Figure 3: Solder joint isothermal stress reduction lines for assemblies with and without underfill.

Application and Verification of the Underfill Model

The underfill model was applied to a silicon on ceramic test vehicle for which moiré displacements fields were measured by B. Han et al. [14]. Young's modulus for the underfill material (E_U) was not known so the model was run for values of E_U typical of existing materials (E_U = 0.9, 1.4 and 2.0 Mpsi). Thermal loading was ΔT = -80°C from 102°C to room temperature.

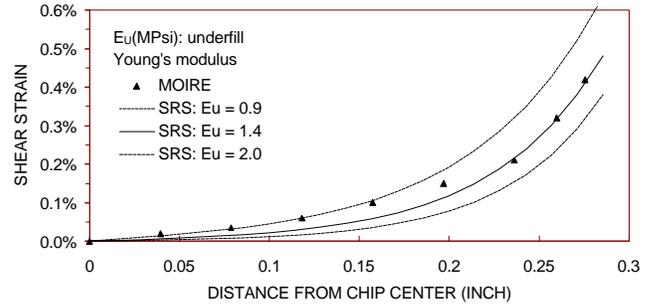Figure 4: Shear strain distribution in underfill layer of silicon-on-ceramic test vehicle (ΔT = -80°C).

The predicted shear strain distribution in the underfill layer, from the center to the edge of the chip, is plotted in Figure 4. Average shear strains from moiré measurements are shown as triangles. The trend of predicted strains agrees with the data. In the high strain region towards the edge of the chip, the model fits best for E_U = 1.4 Mpsi. Sources of discrepancy include simplifications inherent to the strength of materials approach, uncertainties in material properties, the possible temperature dependence of underfill properties, and the absence of end fillet effects in the model. The resolution of measured displacements and the approximation of displacement cross-derivatives for strain calculations may also contribute to the discrepancy, especially in the low strain region. The agreement between predictions and experiment is good and gives support to use of the model for further parametric studies. The strain reduction factor, R, and the resulting effective CTE mismatches, $\Delta\alpha/R$, are given in Table 1 for the three assumed values of E_U.

Table 1: Strain Reduction Factors, R, and effective CTE mismatch, $\Delta\alpha/R$, for Various Values of Underfill Modulus, E_U

E_U (Mpsi)	R	$\Delta\alpha/R$ (ppm/°C)
0.9	5.04	0.83
1.4	6.64	0.63
2.0	8.42	0.50

As E_U increases, the underfill layer provides increased coupling between the chip and substrate and the strain reduction factor increases from 5.04 to 8.42. The solder joints see an effective CTE mismatch under 1 ppm/°C, over five times less than the CTE-mismatch of the assembly without underfill ($\Delta\alpha = 4.2$ ppm/°C for silicon on alumina).

Underfill Delamination

The underfill model is applied to FCOB test vehicles from experiments conducted by O'Malley et al. [15]. The reader is referred to [15, 16] for a description of test vehicles, test conditions and failure analysis. Underfill delamination was the primary failure mode during air cycling and Liquid-to-Liquid Thermal Shock (LLTS) from -55 to 125°C. Model input parameters for boards and assemblies from the three vendors A, B and C [15] are given in Table 3. Parameters in bold are from [15], with thickness of the underfill layer taken as average gap heights (Figure 11 in [15]). Other parameters, including Young's modulus of the underfill material, were given nominal values. Vendor differentiating parameters in Table 2 are the board CTE, Young's modulus and the underfill layer thickness. The chip DNP was L = 0.187".

Table 2: FCOB Test Vehicle Dimensions and Material Properties.

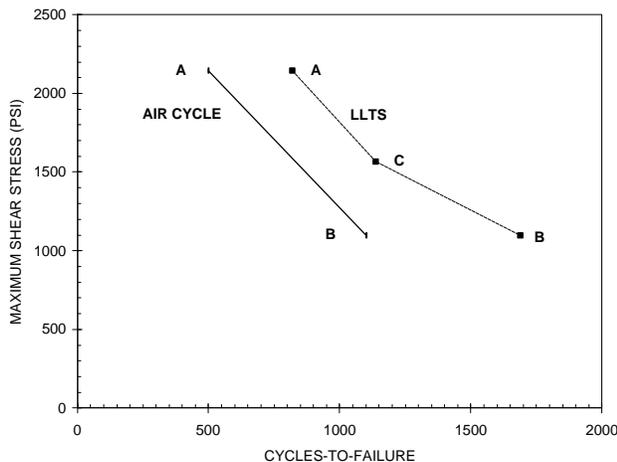|	thickness (mil)	Young's modulus (Mpsi)	Poisson's ratio	CTE (ppm/°C)
silicon die	**20**	29	0.3	2.8
vendor A:				
board	**18**	**0.652**	0.3	**18.8**
underfill	**4.6**	1.0	0.28	NA
vendor B:				
board	**18**	**0.290**	0.3	**18.6**
underfill	**5.5**	1.0	0.28	NA
vendor C:				
board	**18**	**0.319**	0.3	**23.1**
underfill	**4.2**	1.0	0.28	NA

Figure 5: Maximum shear stress versus cycles-to-failure.

Figure 5 shows that the calculated maximum shear stresses follow trends in cycles-to-failure for the three assembly types and two test conditions. The LTTS data is the average of cycles to initial failure from eight lots that were tested over a period of eight months (Figures 6 to 8 in [15]). For boards from vendor C, the data is averaged over the first three lots since performance was observed to degrade after three months due to process related issues. The air cycling data for test vehicles type A and B is from Figure 10 in [15]. Data for type C test vehicles is not included because the air cycle was conducted after performance degradation for type C boards was noticed. The difference between air cycling and LTTS is attributed to the statistical nature of cycles-to-failure, with the LTTS data being averaged over several lots and the air cycling data being from a single lot, as well as differences in dwell times (5 minutes for LTTS, 20 minutes for air-to-air). The correlations in Figure 5 cannot be used directly for predictive modeling since the model does not capture the dynamics of delamination failures. However, since solder joint failures are thought to occur in a short period of time after underfill delamination begins, the calculated maximum shear stress can serve as an indicator of delamination risk in comparative studies looking at changes in design parameters and/or material properties.

Underfill Parametric Studies

As an application of the underfill model, parametric studies are conducted for a generic assembly with a 15 mil thick die on 62 mil thick FR-4 ($E_2 = 2.5 \times 10^6$ psi, $\nu_2 = 0.28$, $\alpha_2 = 16$ ppm/°C). The underfill thickness is 4 mil.
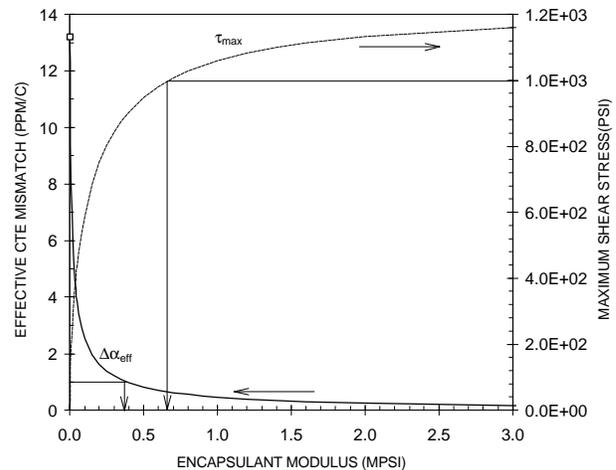

Figure 6: Effect of underfill modulus on effective CTE mismatch and maximum shear stress.

Figure 6 shows the effective CTE mismatch and maximum interfacial shear stresses ($\Delta T = 100$°C) as a function of the underfill modulus for a 10 mm square (L = 0.278") die. For $E_U = 0.4$ Mpsi, the effective CTE mismatch is less than 0.975 ppm/°C. Since the CTE mismatch for the bare chip assembly is 13.2 ppm/°C, the strain reduction factor is R = 13.5. As the modulus increases, the strain reduction factor increases further and so does the maximum shear stress. Curves like those shown in Figure 6 are of use to determine a range of underfill moduli for a given application. For example, if an effective CTE mismatch of 1 ppm/°C is required to meet solder joint reliability goals, and if the maximum interfacial shear stress is to stay below 1000 psi to meet interfacial strength requirements, then the underfill modulus should be in the range 0.37 Mpsi to 0.65 Mpsi.

Figure 7 shows die size effects for a fixed value of the underfill modulus. For die sizes in the range 5 to 20 mm square, an underfill material with

modulus $E_U = 0.7$ Mpsi provides enough stiffness to reduce the CTE mismatch from 13.2 ppm/°C to an effective mismatch of 1.2 ppm/°C or less.
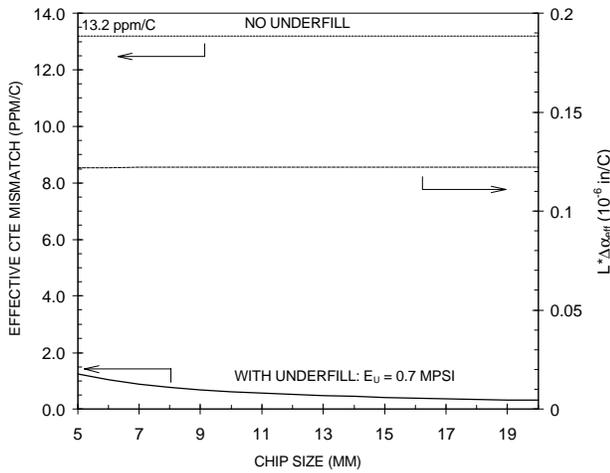

Figure 7: Chip size effects.

The effective CTE mismatch decreases as the chip size increases since a larger chip provides a larger underfill coupling area. However, the thermal expansion mismatch per unit of temperature change, given by $L*\Delta\alpha_{eff}$ on the secondary axis of Figure 7, remains about constant and the underfill layer is effective in decoupling the die from the board independent of die size. A similar conclusion was reached by Tsukada [17] based on more detailed finite element studies.
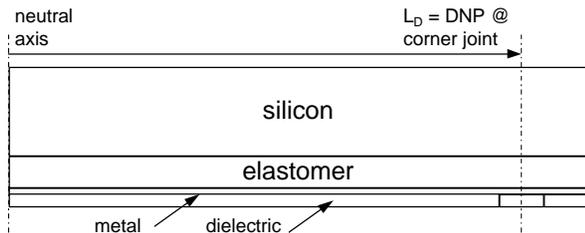
MICRO-BGA MODEL

Figure 8: Schematic of micro-BGA package model.

Figure 8 is a schematic of half of a micro-BGA package, where a low modulus compliant elastomer layer provides for decoupling between the silicon die and the package substrate (metal layers + dielectric). During thermal cycling, the compliant elastomer layer, with a Young's modulus of a few hundred psi, is essentially in shear. Shear is driven by the CTE mismatch between the die and the package substrate, as well as external forces and moments that the solder joints exert on the package.

Figure 9 shows the shear stress distribution, $\tau(x)$, in the elastomer layer, forces and moments exerted by the solder joints (F_{joint}, M_{joint}) and internal forces and moments ($P_i(x)$, $M_i(x)$) in a vertical cross-section of the package. Stresses and strains in the micro-BGA package are solved for by using existing theories of multilayer stacks and adhesive bonds. The solution follows steps similar to the mechanical analysis of flip-chip assemblies with underfill. Details of the model will be presented in [18]. The effective package CTE that is seen by the solder joints is derived from calculated strains on the bottom side of the package. For assembly stiffness calculations, the stretching and bending stiffness of the package are obtained as functions of chip size, geometry and material properties of the different layers of the package.
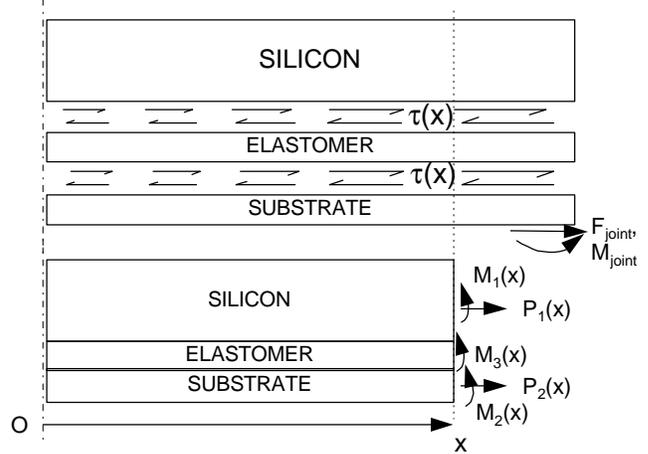

Figure 9: Internal stresses in micro-BGA package.

The micro-BGA model was applied to a generic micro-BGA mounted on a 0.062" FR-4 board and with a 15 mil thick die. Material properties that were used are from [19]. Figure 10 shows the effective package CTE and assembly stiffness as a function of thickness of the compliant elastomer layer. The effective package CTE increases and the assembly stiffness decreases as the elastomer thickness increases. The elastomer layer has to be thick enough to provide an effective package CTE that is close to the CTE of FR-4 boards. For a thickness of 6 mil, the effective CTE is in the range 15.7 ppm/C (10 mm die) to 14.5 ppm/C (15 mm die). Beyond 6 mils, incremental gains in effective CTE and assembly compliance are limited. Nevertheless, with a minimum thickness of the compliant elastomer, the package-to-board CTE mismatch and the assembly stiffness are greatly reduced when compared to the situation of bare chips on FR-4.
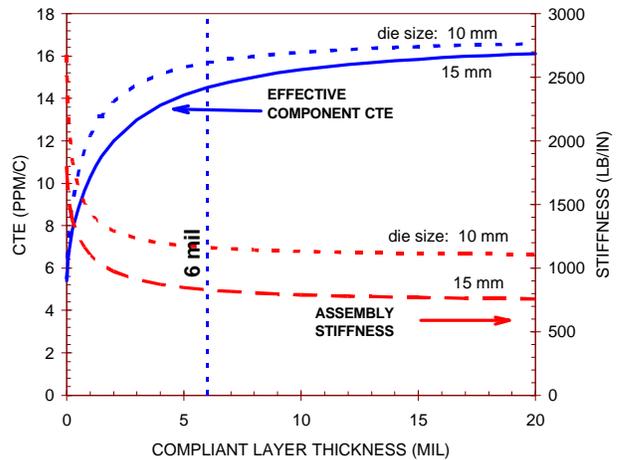

Figure 10: Micro-BGA effective CTE and assembly stiffness as a function of elastomer layer thickness.

Results of the above parametric study are in agreement with the conclusions of finite element studies in [19, 20] and suggest that the micro-BGA model quantifies the chip-to-board decoupling well. As with PBGAs, there is a

chip size effect, the impact of which, as well as other parameters, have to be evaluated on a case-by case basis. Further verification of the micro-BGA model will be conducted as assembly reliability data becomes available.

DESIGN APPLICATION

In this section, we apply the previous CSP models to compare the attachment reliability of bare die, flip-chip with underfill and micro-BGA for a given use environment.

A 10 mm square, 15 mil thick silicon die is to be mounted on 0.062" FR-4 with an in-plane CTE of 18 ppm/ºC. The board is for use in an outdoor cabinet where the assembly experiences a daily temperature swing between 25ºC and 55ºC with long dwells of 710 minutes at the temperature extremes. The question raised by the design team is: "What is the attachment reliability for the three choices of CSP technologies: bare die, Direct Chip Attach (DCA), i.e. flip-chip with underfill, and micro-BGA?"

The data input screens for the bare die assembly (11 parameters), flip-chip with underfill (15 parameters) and for the micro-BGA package (23 parameters) are shown in Figures B.1 to B.3 (appendix B). Material properties are assigned nominal values from the literature. For the three technology options, assembly parameters are assumed to be the same, with a nominal package stand-off of 5 mil. The underfill material has a Young's modulus of 2 Mpsi and the 6 mil thick elastomer layer of the micro-BGA package has a modulus of 1000 psi.
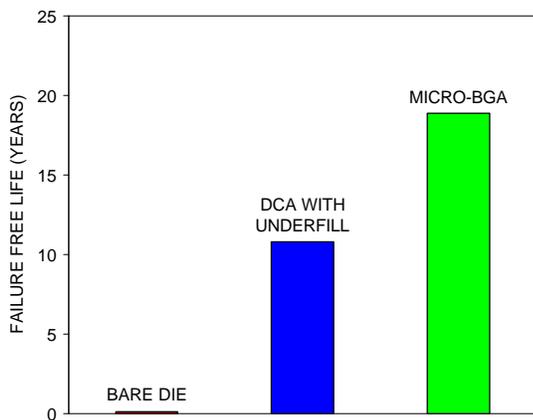

Figure 11: Application-specific attachment reliability predictions for three CSP technologies.

Figure 11 shows SRS attachment reliability predictions given as failure-free times in the field. As expected, the bare die assembly has a very short life, less than two months. Attachment reliability is greatly improved for the other two technologies, with failure free lives greater than 10 years for DCA with underfill and over 18 years for the micro-BGA assembly. It is important to note that the above predictions are application dependent and results will change for another set of design parameters and material properties. However, since the model computations are quick (a few seconds on a low-end personal computer), parametric studies can be conducted rapidly for other combinations of materials, geometry, and use conditions.

CONCLUSIONS

Strength of materials models have been developed in an attempt to capture the effects of die/board interaction on CSP attachment reliability. Model input includes from one to two dozen parameters depending on the package type. This makes material characterization an important aspect of the life prediction process since material properties are process dependent and are not always available in industry standards.

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APPENDIX A: FLIP CHIP WITH UNDERFILL MODEL

We use a strength of material approach to quantify the mechanics of flip-chip assemblies with underfill. For simplification, we only model a slice of the assembly of width the assembly pitch, P, in the diagonal direction of the die. The model assumes that the die and substrate have different in-plane CTEs and that the CTE of the underfill material is close to that of solder. That is, in-plane thermal expansion mismatch, which is accommodated in part by stretching and bending of the assembly, is the primary driving force for solder joint deformations but the joints are not stretched in the out-of-plane direction.

Model Formulation

Solder joints are subject to shear forces and moments at the joint/die and joint/substrate interfaces as in Hall's model of Leadless Ceramic Chip Carrier (LCCC) assemblies [12]. The stress/strain solution in the underfill assembly is obtained by applying Suhir's theory of adhesive bonds [13] to a tri-layer assembly subject to a temperature swing ΔT^1 *and* external forces and moments that arise from the solder joint connections. In general, the underfill layer has higher axial compliance than the die and substrate because of the lower modulus of the encapsulant and/or the smaller thickness of the underfill layer. Under those conditions, and when the substrate is not CTE-matched to the die, Suhir [13] showed that the mechanical response of the assembly is independent of the CTE of the adhesive material and that the adhesive layer is in shear. Thus, we can neglect thermal strains in the underfill and coupling between the die and substrate is controlled by shear stiffness of the underfill layer.
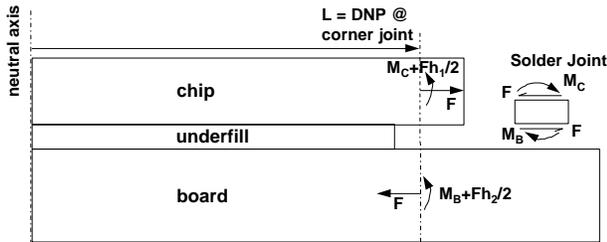

Figure A.1: Free body diagrams of solder joint and tri-layer stack.

Figure A.1 shows free-body diagrams of the substrate/underfill/die tri-layer assembly and of an outer-most corner joint at a distance L from the neutral axis. During thermal cycling, shear forces, F, and moments, M_C at the top and M_B at the bottom, arise at the solder joint interfaces. The free-body diagram of the tri-layer assembly (Figure 2) without solder joints shows

equivalent forces and moments on the mid-plane of the die and substrate of thickness h_1 and h_2, respectively. Equilibrium of moments for the solder joint gives:

$$M_C + M_B = Fh_U \tag{A1}$$

where h_U is the solder joint height or the thickness of the underfill layer. The solder joint shear strain is:

$$\gamma = \frac{U_B - U_C}{h_U} - \frac{L}{\rho(L)} \tag{A2}$$

where U_B and U_C are x-axis displacements of the solder joint at the substrate and chip interfaces. The first term on the right hand side of (A2) is the angle of in-plane shear, the second term is the angle of solder joint distortion due to bending of the assembly with a radius of curvature $\rho(L)$ at $x = L$.
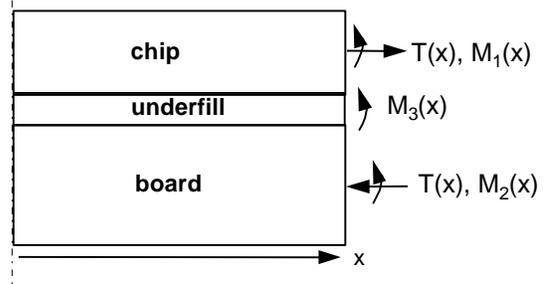

Figure A.2: Forces and moments at a cross-section x of the assembly.

Figures 2 and A.2 show the assumed distribution of interfacial shear stresses, $\tau(x)$, and internal traction forces and moments, $T(x)$ and $M_i = M_i(x)$, in the tri-layer assembly[2]. Traction forces in the die and substrate are self-equilibrating because the underfill layer is in shear and does not carry traction loads. The x-displacements at the bottom of the die and at the top of the substrate are:

$$u_1(x) = \alpha_1 \Delta Tx + \frac{\lambda_1}{P} \int_0^x T(\xi)d\xi - \kappa_1 \tau(x) + \frac{h_1}{2} \int_0^x \frac{d\xi}{\rho(\xi)} \tag{A3}$$

$$u_2(x) = \alpha_2 \Delta Tx - \frac{\lambda_2}{P} \int_0^x T(\xi)d\xi + \kappa_2 \tau(x) - \frac{h_2}{2} \int_0^x \frac{d\xi}{\rho(\xi)} \tag{A4}$$

where λ_i and k_i (i = 1, 2) are axial and shear compliance factors, h_i and α_i are the layers thickness and CTEs, and $\rho(x)$ is the length-dependent curvature of the assembly. To a first order, the compliance factors are $\kappa_i = h_i /(3G_i)$ for i = 1, 2, $\lambda_1 = (1-\nu_1)/(E_1 h_1)$, $\lambda_2 = (1-\nu_2^2)/(2 E_2 h_2)$ where E_i, G_i and ν_i are Young's, shear moduli and Poisson's ratios. The λ_2 formulation attempts to capture two-dimensional effects and assumes that the substrate can be treated as an axi-symmetric, infinite plate as in Hall's model of LCCC assemblies [12]. The axial compliance of the underfill layer is $\lambda_U = (1-\nu_U)/(E_U h_U)$ where E_U and ν_U are Young's modulus and Poisson's ratio of the underfill material. The condition $\lambda_U \gg \lambda_1$, λ_2 must be met for the model to apply. The die and substrate displacements are accommodated by shear of the underfill layer, thus:

$$u_1(x) - u_2(x) = \kappa_U \tau(x) \tag{A5}$$

where $\kappa_U = 2 h_U / (3 G_U)$ is the compliance factor of the underfill layer in shear [13]. From equilibrium of forces and moments:

$$T(x) = F + Pq(x) \tag{A6}$$

$$M_1 + M_u + M_2 = HT(x) + (M_C + F\frac{h_1}{2}) + (M_B + F\frac{h_2}{2}) - FH$$
$$= HT(x) \tag{A7}$$

---

with $q(x) = \int_{-L}^{x} \tau(\xi)d\xi$ and $H = \dfrac{h_1}{2} + h_u + \dfrac{h_2}{2}$. The last three terms on the right hand side of (7) cancel out because of equation (A1). The elastic moment per unit width of the assembly slice is:

$$\frac{D}{\rho(x)} = (M_1 + M_u + M_2)/P \tag{A8}$$

where D is the sum of flexural rigidities: $D = D_1 + D_U + D_2$ where $D_i = \dfrac{E_i h_i^3}{12(1-\nu_i)}$ for i = 1 or U, and $D_2 = \dfrac{E_2 h_2^3}{6(1-\nu_2^2)}$. The rigidity factors are formulated as in Hall's model of LCCC assemblies [12] with the equation for D_2 assuming a substrate of infinite size. From equations (A6) to (A8), the curvature of the assembly at any position x is:

$$\frac{1}{\rho(x)} = \frac{H}{PD} T(x) \tag{A9}$$

At x = L, T(x) = F and $\dfrac{1}{\rho(L)} = \dfrac{FH}{PD}$. After substitution of (A6) and (A9) into (A3) and (A4), and of the latter two equations into (A5), the problem is reduced to the following integral equation for $\tau(x)$:

$$\tau(x) - k^2 \int_0^x q(\xi)d\xi = \left(k^2 \frac{F}{P} - \frac{\Delta\alpha\Delta T}{\kappa}\right)x \tag{A10}$$

where $\Delta\alpha = \alpha_2 - \alpha_1$ and the eigenvalue k is given by: $k^2 = \dfrac{\lambda}{\kappa}(1+f)$,

with $\lambda = \lambda_1 + \lambda_2$, $\kappa = \kappa_1 + \kappa_U + \kappa_2$, $f = \dfrac{hH}{\lambda D}$ and $h = (h_1 + h_2)/2$.

Solution

The solution of (A10) is:

$$\tau(x) = \left(k\frac{F}{P} - \frac{\Delta\alpha\Delta T}{k\kappa}\right)\frac{\sinh(kx)}{\cosh(kL)} \tag{A11}$$

which satisfies the end moment and traction boundary conditions in each layer of the underfill assembly. Having the shear stress solution in the underfill layer, and using equations (A3) to (A9), we can calculate forces, moments, stresses, strains, curvature and displacements in any cross-section of the assembly. Compatibility of displacements at the solder joint interfaces gives: $U_B = u_2(L)$ and $U_C = u_1(L)$ as linear functions of F and ΔT, which we then substitute, along with the above equation for $\rho(L)$, into equation (A2). We obtain the following equation of the solder joint stress reduction line at a given temperature T in the force versus strain (F-γ) plane:

$$h_U\gamma + \frac{F}{K_U} = \frac{1}{R}L\Delta\alpha\Delta T \tag{A12}$$

where the assembly stiffness, K_U, is given by:

$$\frac{1}{K_U} = \frac{L}{P}\left[\left(\lambda + \frac{hH}{D} - k^2\kappa_{12}\right)\frac{\tanh(kL)}{kL} + \frac{h_U \cdot H}{D}\right] \tag{A13}$$

with $\kappa_{12} = \kappa_1 + \kappa_2$. The strain or CTE mismatch reduction factor, R, is:

$$R = \frac{1}{\dfrac{\tanh(kL)}{kL}\left(1 - \dfrac{\kappa_{12}}{\kappa}\right)} \tag{A14}$$

Equation (A12) shows that the underfill layer provides strain relief in the solder joints by constraining the expansion of the die and substrate and reducing the actual CTE mismatch, $\Delta\alpha$, to an effective mismatch, $\Delta\alpha$ / R. Equation (A13) for the assembly stiffness parameter is written as:

$$\frac{1}{K_U} = \frac{1}{K_{1,U}} + \frac{1}{K_{2,U}} + \frac{1}{K_{3,U}} - C_U \tag{A15}$$

where:

$$\frac{1}{K_{1,U}} = \frac{\lambda_1 L}{P}\frac{\tanh(kL)}{kL}, \qquad \frac{1}{K_{2,U}} = \frac{\lambda_2 L}{P}\frac{\tanh(kL)}{kL},$$

$$\frac{1}{K_{3,U}} = \frac{LH}{PD}\left(h\frac{\tanh(kL)}{kL} + h_U\right), \quad C_U = \frac{k^2\kappa_{12}L}{P}\frac{\tanh(kL)}{kL}.$$

From (A15), the assembly with underfill has the stiffness of three springs[3] in parallel ($K_{i,U}$, i = 1 to 3), the compliance of which is reduced by a factor C_U due to mechanical coupling of the die and substrate.

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[3]Spring constants are given on a per joint basis.

APPENDIX B: INPUT DATA SCREENS AND MATERIAL PROPERTIES FOR EXAMPLE APPLICATION

Figure B.1: Input data for bare die assembly.

Figure B.2: Input data for flip-chip with underfill assembly.

Micro BGA Assembly

ENTER/EDIT

Component
Outer-most corner joint DNP (inch): 0.278
Pitch (inch): 0.02
Package thickness (inch): 2.370e-2

Board
Thickness (inch): 0.062
Young 's modulus in tension (psi): 2.5e6
Young 's modulus in flexure (psi): 2.5e6
Poisson 's ratio: 0.28

Assembly
Solder joint height (inch): 5e-3
⦿ Single-sided   ◯ Double-sided

ENTER/EDIT MULTILAYER DATA

	Thickness (inch)	Young's mod. (psi)	Poisson's ratio	CTE (/C)
Dielectric film	2e-3	4e5	0.34	17e-6
Metal layer	0.7e-3	17e6	0.35	17e-6
Compliant layer	6e-3	1e3	0.49	180e-6
Silicon die	15e-3	27e6	0.27	2.8e-6

MICRO BGA MULTILAYER STACK

silicon die
Compliant layer
dielectric film
metal layer

MENU
Compute / update stiffness and CTE parameters
E Erase all data
OK
Copy data, assembly stiffness and CTEs into pre-processor.
? Press for instructions
Cancel

STIFFNESS AND CTE RESULTS
Assembly stiffness K (lb/in): 1.449e+03
Board stretching K1 (lb/in): 2.420e+04
Component stretching K2 (lb/in): 1.541e+03
Effective global CTE (/C): 1.560e-05

Figure B.3: Input data for micro-BGA assembly.