A COMPREHENSIVE SURFACE MOUNT RELIABILITY MODEL: BACKGROUND, VALIDATION AND APPLICATIONS

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ABSTRACT
Surface mount reliability test data acquired by several AT&T organizations between 1984 and 1992 have been integrated in a single design-for-reliability tool, the Comprehensive Surface Mount Reliability (CSMR) model. The CSMR analytical, empirical solder joint life prediction model fits AT&T's database with a correlation coefficient ("r") of 0.97. CSMR applies to evolving families of components, substrates and assembly technology, including 25 mil and 0.5 mm pitch perimeter devices and land grid arrays, and supersedes the Figures of Merit (FM) model in our design standards. The technical foundation of CSMR, its on-going validation and related applications are discussed. The CSMR correlation of 28 accelerated tests has been validated by nine additional test datasets, including failure data for surface mount area array packages.

NEED FOR NEW PREDICTIVE CAPABILITY

Qualitative Issues

The thermal expansion mismatch, or global mismatch, between Surface Mount (SM) components and Printed Wiring Boards (PWBs) has long been a reliability concern [1-3]. References 1 & 2 provide extensive reviews of the issues and how they are being addressed by industry. Global mismatch has been resolved, for example, by using packages with compliant leads [4,5] or tailoring the Coefficients of Thermal Expansion (CTEs) of substrates and components [3].

Since the introduction of SM assembly in its technology base, AT&T has conducted extensive accelerated test programs to qualify circuit board assembly technologies for telecommunication applications. A large test database has been developed with contributions from several test organizations and locations. While the early focus was on resolving the issue of global mismatches, reliability testing of evolving assembly technologies has shown that the thermal expansion mismatch between solder and the lead frame or PWB, referred to as local mismatches, is also a significant factor with most compliant lead assemblies. When global mismatch is eliminated by design, local mismatch remains as the driving force and, although small in general, it is a reliability determining factor. This first became apparent while thermal cycling Alloy 42 SOT (Small Outline Transistor) packages on FR-4 circuit boards [6] and was later confirmed by controlled experiments and analysis [7, 8]. Solder joints of small SOT packages failed much earlier than expected during accelerated thermal cycling and failures were attributed to the large CTE mismatch between 60 Sn - 40 Pb solder (CTE ~ 24 ppm/°C) and Alloy 42 leads (CTE ~ 5 ppm/°C) [6]. The solder to Alloy 42 CTE mismatch was also reported as a contributing factor in Alloy 42 leaded TSOP (Thin Small Outline Package) assemblies [9].

Looking at technology trends, package designs and assembly processes evolve quickly and will keep on evolving (e.g.: ultra fine pitch assembly, area array packages). We thus recognized that empirical solder joint fatigue models developed for first generation surface mount technology need to be validated before they can be applied to later generation technologies.

Modeling Issues

We have correlated fatigue life predictions from several models to failure statistics from our SM reliability database and found that predictive tools such as the AT&T's Figures of Merit [10] and their derivatives [11] are too conservative or erroneous when applied to the latest assembly technologies [9, 12]. Predictions over the full spectrum of technology attributes and test conditions in the database can be significantly off. Figures 1 to 2 show the correlation of test results versus model predictions over a wide range of test vehicles and test conditions. Cycles-to-failure are characteristic lives of Weibull failure distributions where solder joint electrical failures were recorded under in-situ continuous monitoring. The diagonal lines in the correlation plots represent what would be a perfect fit between the test data and a model with a correlation coefficient equal to 1.

Figure 1 shows predicted cycles-to-failure from AT&T's old FMs versus test cycles-to-failure. The correlation

coefficient ("r") for Figure 1 is 0.40, which is poor. Most of the leaded chip carriers data are at a departure from the diagonal line. Only leadless devices appear to be reasonably predicted as global mismatch is the governing factor for leadless assemblies and the FM tools were fit mostly to leadless carriers data. Cyclic life predictions for leaded assemblies with copper or Alloy 42 lead frames can be off by orders of magnitude. Figure 2 shows predicted cycles-to-failure from the modified FMs [11] versus test cycles. Although the modified FMs are an attempt at capturing dwell time and average temperature effects, their correlation coefficient over our database is even lower at 0.15. The poor correlation of FMs over the current database is attributed to the fit of these models to a limited set of first generation SM reliability data. Caveats for the FMs [10, 11] preclude their application to more recent and emerging assembly technologies without further verification.

The FMs limitations that had to be overcome to handle the latest technology attributes are as follows:

- FMs address solder fatigue due to global mismatch. Local mismatches are not accounted for.
- Conservatism was built in by assuming complete stress relaxation for field thermal cycling conditions. The cyclic damage as measured by hysteresis loop areas can be significantly overestimated.
- The original models were developed for 25 to 50 mil pitch leadless ceramic chip carriers and 50 mil pitch leaded components with copper leads. Today's SM pitch goes down to 20 mil and 0.5 mm pitch, or less. Alloy 42 is also used as a lead frame material in many packages. Joint and fillet sizes are design and process dependent and have been found to be governing factors [13]. Size effects become even more important as technology moves towards finer pitch assembly and smaller solder joints.

Figure 3 shows the correlation plot of predicted versus test cycles as obtained with the CSMR model [14]. The correlation coefficient is 0.97 and the statistical spread of the data is two to three times about the diagonal line. This spread is typical of fatigue data [13] and a tighter spread is thought improbable given the extent of parameters in the database and the multiplicity of assembly locations and test organizations involved.

SCOPE OF MODEL AND DATABASE

CSMR Model

The CSMR model is an analytical/empirical solder joint life prediction model with robustness over our entire SM reliability database [14]. The model covers three orders of magnitude in cyclic lives and evolving families of components, substrates and assembly technologies. Test conditions include thermal and power cycling over a wide range of frequency and temperature limits.

Four attributes of the model are key to the CSMR correlation and improved our predictive capability over the original Figures of Merit:

- The contribution of local mismatches (solder versus lead frame and solder versus substrate) to cyclic, cumulative damage.
- The use of cyclic, inelastic strain energy as a measure of fatigue damage for both leadless and leaded assemblies.
- A more physically correct constitutive model for solder, including temperature-dependent, fast plastic flow and time/temperature-dependent creep.
- The use of cycles-to-failure per unit area as a scaled measure of cyclic life. The solder crack area which varies over a wide range with packaging and assembly technology serves as a life scaling factor. Crack areas across all test vehicles in our database vary by a factor over 15 times.

Significant results are:

- Cyclic life data from 28 accelerated tests conducted from 1984 to 1992 correlate with cyclic inelastic strain energy within a factor of two to three times. When exercised over the entire database, the new model has a correlation coefficient of 0.97, compared to 0.40 or less for existing models.
- The ensuing formulation of acceleration factors and design-for-reliability rules include the effect of local and global mismatches, plus plastic flow and time-dependent solder creep.
- The new design rules have robustness over new assembly technologies, including large 25 mil pitch packages [12], 0.5 mm pitch Alloy42 and copper leaded TSOPs [9, 15] and ball grid array packages [16, 17].

The CSMR approach has been tested and exercised since mid-1992 and supersedes the FM tools in AT&T's design standards. The model provides added design flexibility, and more accurate, less conservative results than previous models. CSMR is used for physical design, early assessment of new packages and emerging assembly technologies, and the development of faster qualification programs.

SM Reliability Database

The database the original CSMR model is fitted to includes 28 qualification experiments conducted by four test groups at three locations between 1984 and 1992 and funded by several research and design organizations. Test vehicles were assembled at several development centers and factories. All test vehicles were wired and daisy-chained for in-situ continuous monitoring of solder joint electrical continuity. The design and monitoring of test vehicles followed guidelines similar to the IPC's (The Institute for Interconnecting and Packaging Electronic Circuits) [11]. Examples of test vehicle designs, test

procedures and data analysis are given in [4, 6, 9, 12, 15, 18, 19].

Test conditions include power and thermal cycling over a wide range of:

- Frequencies: 10, 15, 24, 48, 60, 72, 96 and 100 cycles/day.
- And temperature swings: 25 to 65°C, 25 to 85°C, 30 to 82°C, 20 to 100°C, 0 to 100°C, -20 to 125°C.

The spectrum of technology attributes in the database covers the following:

- Eutectic or near-eutectic tin-lead solder. Processes are wave-soldering, infra-red, belt and vapor phase reflow at various assembly locations.
- Evolving families of component and packaging technology: discretes (size 1206 and cylindrical resistors); leadless and leaded chip carriers: ceramic leadless carriers, SOT, SOIC (Small Outline Integrated Circuit) , PLCC (Plastic Leaded Chip Carrier), clip lead ceramic carriers, PQFP (Plastic Quad Flat Pack), TSOP, PolyHIC (Polymer Hybrid Integrated Circuit) and others. Component CTEs are in the range 5.4 to 21 ppm/°C.
- Lead frames: copper and Alloy 42.
- Device pitch: 50 to 25 mil; 0.5 mm.
- Substrates: double-sided rigid and multi-layer boards; FR-4 based with CTEs in the range 15 to 21 ppm/°C; or low expansion copper clad invar (CTE ~ 9 ppm/°C) and Kevlar-reinforced boards (CTE ~ 6 ppm/°C).

The CSMR model and reliability database cover a much wider scope of parameters than the existing FMs [10]. The recent extension of CSMR to ball grid array packages [16, 17] shows a very good fit to accelerated test results. As new and emerging technologies are added to the database, test results are also checked against the CSMR model. Solders other than near-eutectic tin-lead have not been qualified to date and our database needs be expanded before we can scale the CSMR model to new solder materials and assembly processes.

CSMR TECHNICAL FOUNDATION

Global and Local CTE Mismatches

Figure 4 is a schematic of a solder joint interconnection between a leaded package and the substrate to which it is attached. *Global mismatch* refers to the overall *shear* deformations of solder joints due to thermal expansion/contraction differentials between the SM package and the substrate. The maximum available shear strain at a corner joint is:

$$\gamma_{avail} = \frac{L_D \Delta\alpha_G \Delta T}{h} \qquad (1)$$

where L_D is half the diagonal dimension of the package; h is the average solder joint height (approximated as half the solder paste thickness, unless otherwise specified); $\Delta\alpha_G$ is the absolute value of the package to substrate "global" CTE mismatch; ΔT is the cyclic thermal fluctuation between low temperature, T_{low} , and high temperature, T_{high} .

Local mismatch refers to *tensile* deformations in the solder joint due to lateral expansion/contraction differentials between solder (~24 ppm/°C for near-eutectic tin-lead) and the lead frame or device material (~ 17 ppm/°C for copper leads, ~ 5 ppm/°C for Alloy 42 leads) or between solder and the substrate material (in the range 15 to 21 ppm/°C for FR-4, ~ 6 ppm/°C for Kevlar-reinforced boards), similar to deformations in a bimetallic strip. Local CTE mismatches with copper mounting pads are not accounted for as their small thickness (about 1 mil) does not contribute much to the lateral stiffness of the lead foot/joint/PWB composite. The maximum available local strain is a normal strain:

$$\varepsilon_{avail} = \Delta\alpha_L \Delta T \qquad (2)$$

where $\Delta\alpha_L$ is the absolute value of the CTE mismatch between solder and the lead frame material, or solder and the PWB material. Local CTE mismatches, lead versus solder and solder versus substrate, are assumed to be de-coupled because of the compliant nature of the solder layer and are thus accounted for separately.

Fatigue Damage Due to Global and Local Mismatches

The CSMR model uses one-dimensional structural models to estimate solder joint stress/strain hysteresis due to *global and local CTE mismatches* during thermal cycling. Premises of the structural models have been presented before [7, 14] and our approach to quantify cyclic stresses and deformations due to global mismatch is similar to that followed by others [20-25]. The same methodology has been expanded to quantify local mismatch effects. CSMR also uses a more physically correct and complete solder model than the Figures of Merit, including elastic deformations, time-independent, fast rate plastic flow, steady state creep, and their thermal dependencies. The fast rate, plastic flow relationship is from stress/strain measurements on SM assemblies [23] and the steady state creep rate relation is from a range of compiled creep data [23, 24], similar to constitutive models used in References 20 and 21.

Following Morrow's generalized fatigue law for metals [26], the cyclic damage imparted to solder joints is the inelastic strain energy estimated as hysteresis loop areas. The strain energy approach to fatigue life predictions applies intuitively to SM assemblies as it allows the addition of cyclic strain energies from local and global mismatches. The application of the above methodology to a variety of test vehicles and the resulting database

correlation indicate that the underlying assumptions are adequate for engineering purposes. A similar strain energy partitioning approach has been proposed in [27] based on hysteresis loops generated by finite element analysis of solder joints in leaded through-hole mounting technology.

The discrepancy in cyclic, inelastic strain energies when complete stress relaxation is assumed at the temperature extremes (as in the FM model) and when creep is accounted for explicitly (CSMR model) can be orders of magnitude [14]. The varying range of strain energy discrepancies suggests that plasticity and creep are a necessary feature of a solder joint life prediction model. The CSMR analysis [14] also illustrates the significant contribution of local mismatches to the total cyclic inelastic strain energies in many SM leaded assemblies. Over a wide range of packages and material parameters, local mismatches can be a small or dominant contributor to total, cyclic inelastic strain energy. Models based on global mismatch cannot predict well for compliant leaded devices which are dominated by local mismatch effects.

Cyclic Life Area Scaling and CSMR Correlation

Another important feature of the CSMR model is the scaling of cyclic life for the solder crack area to account for the effect of solder joint size on the fatigue life. Failure data from 28 accelerated test datasets are correlated in Figure 5 as characteristic cyclic life per unit area versus cyclic, inelastic, strain energy, ΔW_{in}. The cyclic life per unit area is the Weibull characteristic life[1], α, divided by the solder joint crack area, A, in units of cycles/in^2. In general, the area A is approximated by the solder joint load bearing area [10], that is, the area of maximum stress where cracks are most likely to initiate. A was found in the range 2 to 9 x 10^{-4} in^2 for chip carriers, and 23 to 33 x 10^{-4} in^2 for discrete devices in AT&T's database. Failure mode analysis of failed solder joints often is necessary to identify and measure the crack area. On the horizontal axis in Figure 5, the damage parameter or "driving force" is the cyclic, inelastic strain energy ΔW_{in} for global and local mismatches. Except for area scaling, the α/A versus ΔW_{in} correlation is a Morrow's type fatigue law [26]. Several data sets are highlighted in Figure 5:

- Hard failure data from 24 experiments with complete failure statistics. These include: leadless ceramic chip carriers (square symbols), resistors (circles), and leaded devices (diamonds).
- Data shown as triangles pointing upward for four types of leaded devices with no-failure or a single failure at end of test. For this set of data, cycles-to-failure are lower bounds of characteristic lives under test conditions. As these packages had compliant leads, the contribution from global mismatch to total cyclic energy was found to be negligible. The inelastic, strain energy was dominated by contributions from local mismatches.

The 24 hard failure experiments fall in a band that spans about half-an-order of magnitude in cyclic lives (a factor two times below and three times above the central regression line). The scatter of data is typical of fatigue and is judged acceptable given the variety of test vehicles, test conditions and assembly parameters, and given that the test data cover three orders of magnitude along each axis. The four data points with no or only one failure fall on or below the regression line, thus supporting the correlation obtained from hard-failure data and extending it to a lower range of total, cyclic inelastic strain energy.

The scaled cyclic life parameter α/A is interpreted as the number of cycles it takes for a crack or several micro-cracks to grow through a unit of solder attach area. The inverse parameter, A/α , is the 2D equivalent of an average crack propagation rate in metal fatigue. The correlation A/α versus ΔW_{in} would be equivalent to a "da/dN versus J-integral" crack propagation law in fracture mechanics [28] where da/dN is the linear crack growth per load cycle and the J-integral is an energy integral of the stress/strain field around the crack tip. More detailed crack growth phenomenological approaches to solder joint fatigue have been advocated by others [20, 21, 24, 29, 30] and give support to our introduction of the α/A parameter in the correlation of thermal cycling test data.

Crack area scaling to obtain a first order estimate of crack propagation rates is an effective, engineering metric for scaling fatigue lives for a spectrum of components with a wide range of solder joint fracture areas and is the two-dimensional equivalent of the joint length correction factor used by Solomon et al. [13]. The area scaling is empirical and does not attempt to partition fatigue life into crack initiation and crack propagation.

Discussion

Looking at the partitioning of cyclic inelastic strain energy between global and local mismatches across the test database, Figure 5 reflects trends in packaging and assembly technology:

- Global mismatch is dominant for high values of the total cyclic strain energy (lower right region in Figure 5). This dataset consists of leadless chip

[1] $\alpha = N_{63\%}$ = cycles to 1 - 1/e = 63.2% failures, independent of the slope β of the Weibull failure distribution. An average value of β for good quality solder joints is 4 for which $N_{50\%}$ = median cycles to failure = 0.912 α .

carriers with a large global CTE mismatch, that is, early types of SM packages.

- For lower values of the total cyclic inelastic strain energy (upper left region in Figure 5), local mismatches have a dominant effect. All the data in this region are from packages with compliant leads and/or small package to substrate CTE mismatch. For example, PLCCs on FR-4 have almost no energy contribution from global mismatch and PolyHICs on FR-4 have a low 22% energy contribution from global mismatch. For all plastic packages in that region, the package bodies are thick relative to the silicon die, their CTEs are dominated by that of the plastic compound and are close to the substrate CTEs, and package leads are compliant. In other words, the global expansion mismatch has been designed out of these assemblies, thus reducing or eliminating the large global CTE mismatch associated with earlier SM technology.
- There is a transition region where neither global, nor local mismatch are negligible, although global mismatch tends to have more weight. For example, with 1206 discrete resistors on FR-4, the contribution of global mismatch to total energy is 74%, that of local mismatches is 26%. This region also includes Alloy 42 TSOPs on FR-4 where global mismatch becomes important as packages are thinned down. The CTE of these TSOPs is dictated by the low expansion of the silicon die and the Alloy 42 lead frame.

One data point of interest in the database and the CSMR correlation is the SOT-23 with Alloy 42 lead frame. The global thermal expansion mismatch is small and the total energy is dominated by the lead to solder CTE mismatch (about 80% of the total energy). The contribution from global mismatch alone is negligible (~ 0.01% of the total energy). The remaining 20% of the total cyclic strain energy comes from the solder to PWB local mismatch. This confirms conclusions from failure mode analysis that the SOT-23 solder joint failures were attributed to the CTE mismatch between Alloy 42 and solder [6].

The database analysis and the CSMR correlation indicate that design parameters have the most influence on solder joint fatigue. The list of required input parameters to the CSMR model (Appendix A) includes a dozen design parameters, plus thermal history, design life and reliability requirements. No trend was found suggesting a strong effect of assembly processes. The solder micro-structure certainly varies with cooling rates and other process parameters and the scatter of test data within the CSMR correlation bands probably reflect these variations.

VALIDATION OF CSMR MODEL

Figure 6 shows the fit of nine new test datasets to the original CSMR model. The new data points cover more than one order of magnitude along both axes and fit within the scatter bands of the CSMR correlation. The solder joint fatigue data were obtained from the following experiments:

- Alloy 42 and copper leaded TSOPs [15] (four datasets) with devices from two suppliers. Solder fatigue life was five times better for copper compared to Alloy 42 leaded TSOPs.
- Ball Grid Arrays (BGAs) [16, 17] (four datasets) with failures recorded at solder joints near the edge of silicon chips. The CSMR structural analysis was expanded to BGAs where the component CTE and stiffness vary as a function of joint position. Failure times and locations were predicted accurately.
- PLCCs with short joint length [32] (one dataset). Detailed failure analysis of short length "defective" solder joints (35 mil average length versus 50 mil for good quality joints) led to the conclusion [32] that "the most critical joint dimensions are probably joint length and joint width which yields the effective cross-section." This also substantiates the area scaling in the CSMR analysis.

The CSMR correlation of effective crack propagation rates to cyclic inelastic strain energy suggests that, as a first approximation, crack growth proceeds at a constant rate. Fatigue cracks evolve from material coarsening, cavity growth, grain slippage and other complex micro-mechanisms [2], and multiple micro-cracks grow and coalesce [2, 7] into a fractured solder joint. The hypothesis of a single fatigue crack is more likely for stiff assemblies. The cumulative fractured area increases cyclically because of increasing slippage and material/grain separation at the micro-structural level. The growth of the solder crack area (a single crack or several micro-cracks) at a constant rate is strongly supported by strength measurements reported by J. Seyyedi [32]. The pull force of leaded solder joints of several compositions, including eutectic tin-lead, was found to degrade linearly with increasing thermal cycles thus indicating that the solder crack area grew approximately at a constant rate.

As of early 1993, the CSMR correlation is supported by 37 datasets in AT&T's surface mount reliability database. Its validity is checked as new test results and any other solder fatigue information become available.

DESIGN FOR RELIABILITY RULES

Given a solder joint design and anticipated use conditions, reliability goals are stated in terms of an acceptable cumulative failure distribution of at most F at the end of the design life, or N cycles of operations. The wear-out Weibull distribution [33] of solder joint failures

needs to be included in SM assembly life predictions. For known use conditions, N should be less than $N_f(F)$, the number of acceptable cycles to F failures, and the cumulative damage at end of life is defined as:

$$D = \frac{N}{N_f(F)} \quad (3)$$

D should be less than 1 for stated reliability goals to be met. D represents the fraction of available fatigue life or acceptable cycles-to-failure ($N_f(F)$) that have been used up at the end of the design life (N operation cycles).

Assuming a two parameter Weibull distribution, we get:

$$N_f(F) = \alpha \times \left[-\ln(1-F)\right]^{1/\beta} \quad (4)$$

where α, the characteristic life of the field failure distribution is calculated by using the CSMR model. A conservative design rule is to use the lower limit of the CSMR correlation band (Figure 5) to calculate α. The cumulative damage at end of life is thus obtained as:

$$D = \frac{N}{\alpha \times \left[-\ln(1-F)\right]^{1/\beta}} \quad (5)$$

The product thermal history may encompass multiple thermal loads from Environmental Stress Testing (EST), storage and transport cycles, to typical and worst case service conditions. The cumulative fatigue damage is then estimated using Miner's rule [34]:

$$D = \sum_i \frac{N_i}{N_{f,i}(F)} \quad (6)$$

where N_i is the number of operating cycles for each thermal load. For each stress condition i, the number of cycles-to-failure to an acceptable cumulative failure rate F is:

$$N_{f,i}(F) = \alpha_i \times \left[-\ln(1-F)\right]^{1/\beta} \quad (7)$$

with α_i = cycles-to-63.2% failure for stress condition i obtained from the CSMR model. When D is less than 1, the actual cumulative failure probability is less than F and target reliability goals are met. When D is larger than 1, reliability goals are not met. When D reaches 100%, the cumulative failure probability is equal to F. In a situation where D approaches 1, accelerated testing is recommended to validate the solder joint design and capture the effects of variable assembly quality. Parametric use of the CSMR model can also help identify critical design parameters and suggest design changes that will improve reliability margins.

APPLICATIONS
PolyHIC on FR-4
Test Conditions

Applying the CSMR model to PolyHIC[2] accelerated testing [12], median cycles-to-failures on a per device basis are predicted in the range 8400 to 17,000 cycles. The median test cycles on a per device basis was about 10,000 (from $N_{50\%}$ = 15883 on a per octile basis in [12]). Using the modified FMs [11], median test life was predicted at less than 100 cycles. The FM prediction erred on two accounts:

- The cumulative cyclic damage from global expansion mismatch was largely over-estimated under the hypothesis of complete stress reduction at the temperature extremes. The frequency correction factor in the modified FMs [11] only had a slight effect on predicted cycles-to-failure.
- Local mismatches had about 80% weight in the total, cyclic inelastic strain energy under test conditions, an effect that is not accounted for by the FM models.

Use Conditions

For illustrative purposes, consider office use conditions with a 25 year design life, and an instantaneous failure rate for component attachment at the end of service life (t=25 years) assumed at: λ = 0.3 FIT, i.e.: F(25 years) = 1.64 x 10^{-5}. The product thermal environment is shown in Table 1, where N_i is the number of operating cycles for each stress condition (i = 1,6).

Table 1: Office Use Thermal Environment, 25 Year Service Life

Stress (i = 1, 6)	T (°C)			Cycles
	Low	High	ΔT	N_i
1. EST	-20	70	90	20
2. Storage	-20	25	45	25
3. Transport	-40	25	65	25
4. Operations	42	47	5	6725
5. Worst Days	42	52	10	2280
6. AC* failures	45	65	20	50

*AC= Air-Conditioning

For EST conditions (stress testing), we used a worst case soak of 1/2 hour at 70°C (estimated from temperature profile in [35]); for the other service conditions, the dwell at T_{high} was taken as 1/2 day = 720 minutes. The cycles-to-failure, $N_{f,i}$, are given in Table 2 for the assumed target λ = 0.3 FIT per device at 25 years:

[2] PolyHIC is a 244 I/Os, 1.8" square multi-chip package with compliant leads and a large CTE mismatch to the FR-4 board.

Table 2: Cycles-to-Failure and Damage for Each Stress Condition

Stress i = 1,6	Cycles $N_{f,i}$ (F)	Damage: $N_i / N_{f,i}$ (F)
1. EST	657	3.05%
2. Storage	3398	0.74%
3. Transport	1311	1.91%
4. Operations	$1.091\ 10^6$	0.62%
5. Worst Days	$1.727\ 10^5$	1.32%
6. AC failures	$2.435\ 10^4$	0.21%

Using Miner's rule [34], we get:

$$D = \sum_i \frac{N_i}{N_{f,i}(F)} = 7.85\% \qquad (12)$$

As D is much less than 1, the targeted reliability goals are met with a large margin. This is confirmed by field failure rates predicted from test results [12]. Based on FMs, the PolyHIC SM design would not have met reliability goals for the above thermal history.

Optimizing Accelerated Test Conditions

We have also used the CSMR model to optimize thermal cycling test regimens. For example, Figure 7 shows cyclic, inelastic strain energies (global and global + local) as a function of dwell times for a temperature swing between 0°C and 100°C and several types of packages on FR-4 substrates.

For PQFPs with compliant leads, global strain energy increases with dwell times as expected. However, global remains a small fraction of the total strain energy which is dominated by local mismatches. As local mismatch solder deformations are driven by stiff members of the assembly (the lead foot and the substrate in tension), most of the inelastic energy due to local mismatches is imparted as fast rate plastic flow and initial creep rates are very fast. Thus the cyclic cumulative damage as measured by the total cyclic inelastic strain energy has a negligible dwell time dependency.

At the other end of the device spectrum, the response of leadless ceramic chip carrier assemblies (LCCC in Figure 7) is dominated by global mismatch and local mismatch effects are negligible. For global mismatch, LCCCs on FR-4 are a stiff assembly and the associated inelastic strain energy is largely dominated by plastic flow while creep is limited by stress reduction lines with high slopes, high creep rates and rapid stress reduction. The effect of dwell time is also very small as stress reduction is almost complete in minutes.

TSOPs and PolyHICs have intermediate responses and are untypical with mixed contributions from global and local mismatches. The dwell time effect shows for global mismatch as expected with leaded attachment. However, its effect is not significant overall (global + local) and increases in cumulative damage with dwell times are not strong enough to warrant a worthwhile gain in test efficiency, measured in strain energy per cycle or per unit of time. As most devices we qualify are closer to the PQFP or the LCCC type (from the point of view of solder joint reliability), our accelerated tests do not require long soaks at the temperature extremes. Dwell times of a few minutes (about 5 minutes or less) after parts reach thermal equilibrium are long enough and provide reasonable test efficiency for telecommunication applications. Dwells longer than 5 minutes do not yield worthwhile gains and lead to lengthy qualification programs. Our common qualification tests go from 0°C to 100°C at frequencies in the range 48 to 100 cycles/day depending on the chamber temperature ramp rates and the thermal load under test. Faster thermal cycles and larger temperature swings are being investigated [36] as shorter dwells are predicted to be adequate.

The CSMR analysis of dwell times for a variety of components is consistent with test regimen designs reported by others:

- Pao [37] proposed to reduce dwell times from 30 to 3 minutes in cycles from -55°C to 125°C and -20°C to 100°C based on the correlation of micro-structural crack growth analysis to the fatigue life of leadless device solder joints. Propagating cracks were found to show little additional growth during hold times because of rapid stress relaxation and low stress levels at high temperatures and negligible change in creep strains at low temperatures.
- DEC authors [38-40] run Fast Temperature Cycling (FTC) from -10°C to 110°C with 30°C/minute effective ramp rates and 1 minute dwells. The correlation of fatigue data for several types of leaded devices and the analysis of solder joint cross-sections after FTC and slow temperature cycling between 15°C and 100°C with 5°C/minute ramps and 5 minute dwells indicated that failure modes were essentially the same for both test regimens [38].

SUMMARY

The CSMR solder joint life prediction model was developed based on the correlation of 28 accelerated tests in our SM reliability database and has been validated since by nine accelerated test datasets. Further validation based on published reliability data is in progress. The model formulation captures three key parameters that our previous predictive capabilities did not account for:

- Local CTE mismatches between solder and the lead or device material, and between solder and the substrate material.
- Plastic flow and solder creep during temperature soaks.

- The solder joint crack area serves as a life scaling factor.

Local mismatch is a significant life controlling parameter for leaded packages. The combined effects of local and global mismatches are added up in an energy-based fatigue law that is validated by a large set of test data.

The CSMR approach is more powerful and more accurate than the existing FM tools. The accuracy of the database correlation and of the ensuing life prediction capability is a factor of two to three on cyclic lives and failure rates are predicted within one order of magnitude. This is very good for a correlation of reliability test data over three orders of magnitude in cyclic lives and a variety of packaging and assembly parameters.

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APPENDIX A
Input to the CSMR Model

The current default constitutive response in the CSMR model (plastic flow, creep rate and their thermal dependencies) is that of eutectic or near-eutectic tin-lead solder. Solder attachment reliability is dependent on:

- Material properties (device, substrate and solder).
- Geometrical and design parameters (device, substrate and solder joint).
- Field thermal environment.
- Intended use and service life.
- Acceptable failure level

Package drawings, including the lead geometry for leaded packages, solder joint geometry and mounting pad size and layout are required input for the CSMR analysis. The specific parameters that are required to use the CSMR model for design purposes or for the analysis of test failure data are listed below.

Substrate Properties:

- α_{subst} = CTE of substrate in x and y directions. The in-plane CTEs of the substrate and the effective component CTE should be measured to obtain accurate values.
- h_{subst} = thickness of substrate.
- E_{subst} = Young's modulus of substrate.

Component Properties:

- α_{comp} = measured CTE of component in its diagonal direction (or CTEs and Young's moduli of each material in package).

- $2L_D$ = distance between the center lines of the two most distant solder joints of a component. For a perimeter chip carrier, $2L_D$ is approximated as the diagonal dimension of the package. For a discrete component, $2L_D$ is the distance between the midpoints of the terminations.
- h_{comp} = component thickness for a leadless device.
- E_{comp} = Young's modulus of component material for a leadless device.
- K_D = "diagonal" flexural stiffness of component corner-most leads.

Lead Frame Properties:

- α_{lead} = CTE of lead frame material.
- h_{lead} = lead foot thickness.
- E_{lead} = Young's modulus of lead frame material.

Assembly Properties:

- h = solder joint height. For leaded attachment, h is taken as one-half the solder paste stencil thickness.
- A = effective solder joint area in shear, or solder joint crack area, approximated as the minimum solder joint cross-section in a plane parallel to the pad. The better estimate is crack area measurements on failed solder joints.
- α_s = CTE of solder material.

Thermal History:

- N_i = number of thermal cycles with temperature excursion ΔT_i between cold ($T_{l,i}$) and hot ($T_{h,i}$) temperatures during the field life of the circuit pack. Subscript i accounts for multiple thermal loads.
- $T_{l,\,i}$, $T_{h,\,i}$ = temperature extremes (low and high) at the component/joint/PWB for stress condition "i".

Design Life and Reliability Parameters:

- N_{yrs} = intended product design life in years.
- F(t) = the acceptable cumulative failure probability per device at end of life.
- β = shape parameter of the Weibull distribution of solder joint failures. β is obtained from accelerated life tests on test vehicles representative of actual products. β has been found in the range 1 to 8, with values from 3 to 5 more typical, and an average of about 4 across AT&T's database.

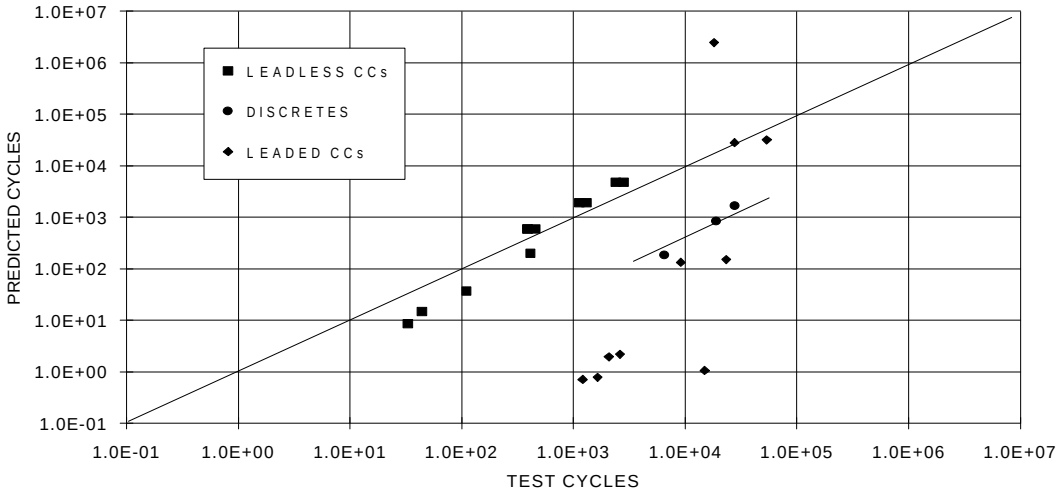

Figure 1: Predicted cycles-to-failure versus test data; AT&T's FM model ("r" = 0.40).

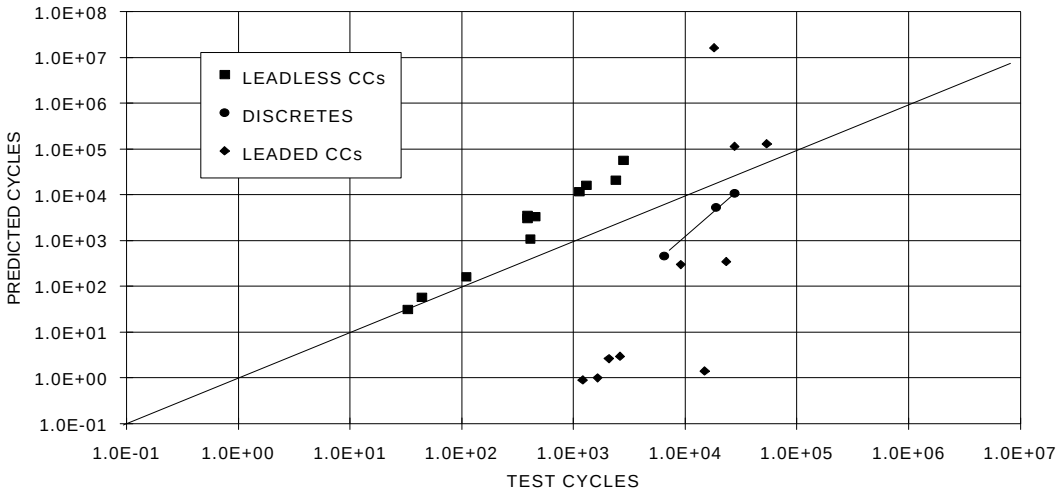

Figure 2: Predicted cycles-to-failure versus test data; modified FM model ("r" = 0.15).

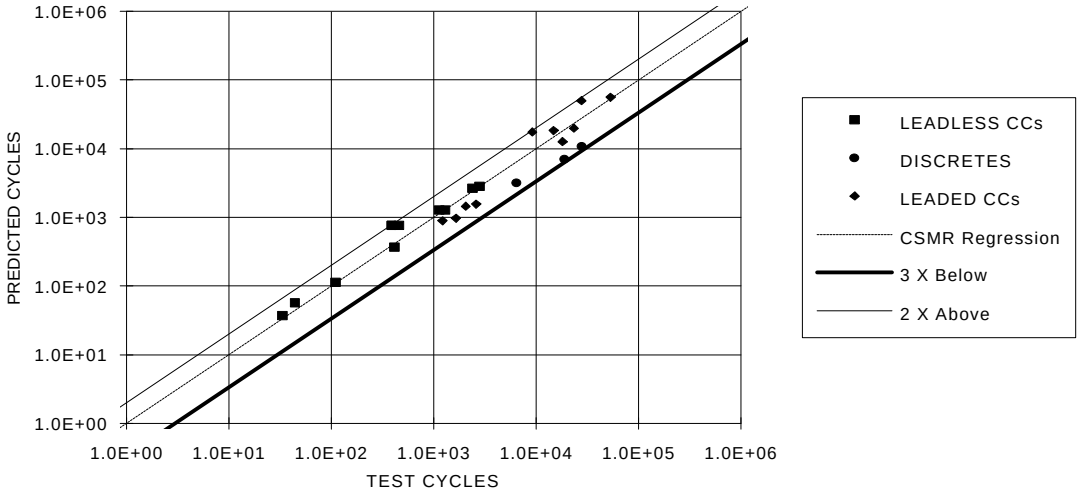

Figure 3: Predicted cycles-to-failure versus test data; CSMR model ("r" = 0.97).

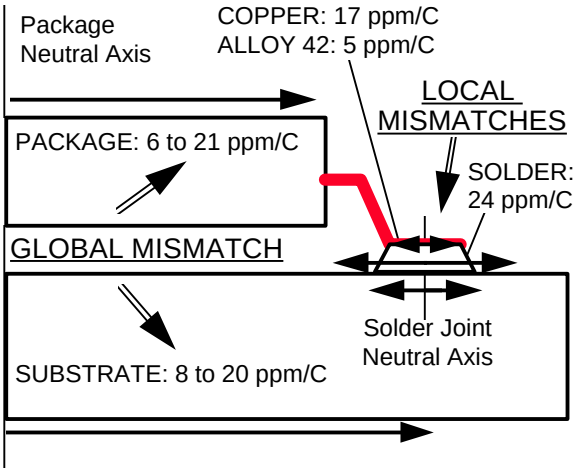

Figure 4: Schematic of SM leaded assembly and reliability driving forces.

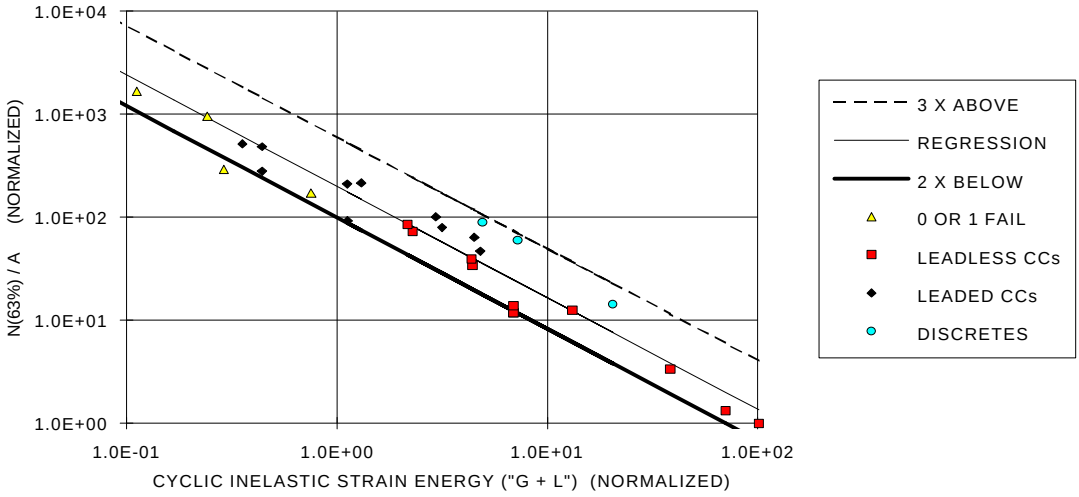

Figure 5: Correlation of CSMR model over AT&T's database (1984-1992).

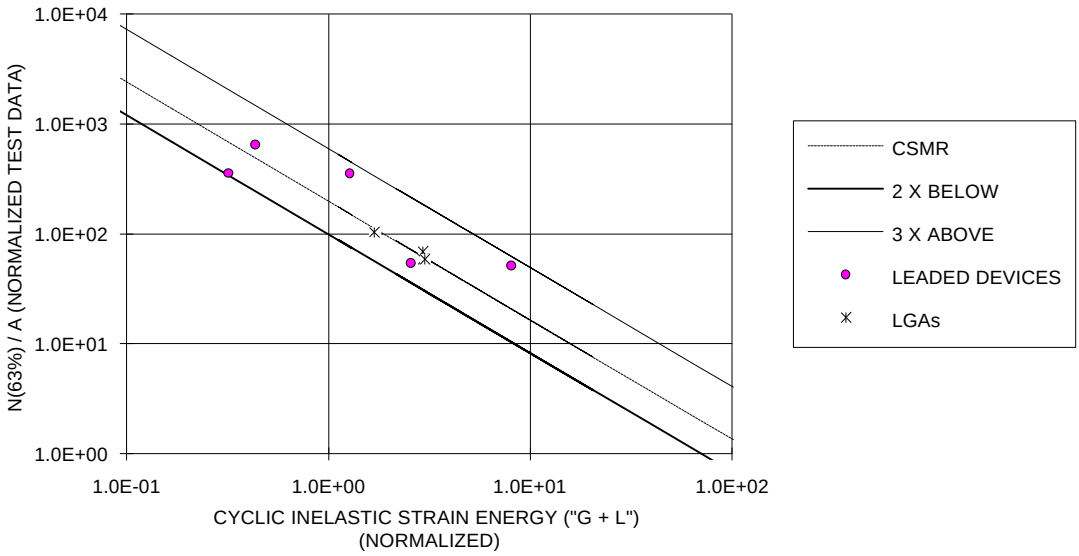

Figure 6: Fit of new test data (9 datasets) to CSMR correlation.

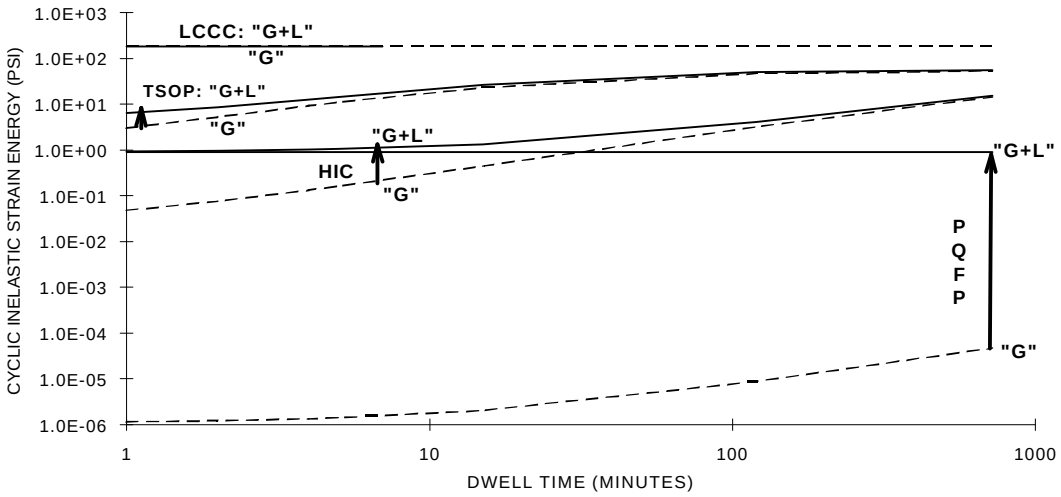

Figure 7: Cyclic inelastic strain energy as a function of dwell times. Global ("G") versus Global + Local ("G + L") for thermal cycling between 0 and 100°C.