FLIP-CHIP / CSP ASSEMBLY RELIABILITY AND SOLDER VOLUME EFFECTS

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ABSTRACT

With accelerated test data suggesting that most flip-chip (FC) and Chip Scale Package (CSP) assemblies on organic boards have shorter lives than conventional or area-array Surface Mount (SM) assemblies, solder joint reliability is possibly being pushed to the limits. The reliability of FC and CSP assemblies cannot be taken for granted, thus requiring careful interpretation of test results and more accurate means of extrapolating test failure cycles to field conditions. This paper presents the extension of the Solder Reliability Solutions (SRS) model [1] to soldered FC and CSP assemblies. The model is validated by failure data from over fifty accelerated thermal cycling tests, including FC, ceramic CSP and micro-BGA† solder joint failures. For FC assemblies, underfill shear strain predictions nicely fit shear strain distributions obtained by moiré interferometry and predicted die stresses are in agreement with stress sensor measurements. Last, the analysis of FC test results demonstrates the impact of solder joint volume on attachment reliability and a solder volume correction factor is introduced in the SRS model. The effect of solder volume on solder joint fatigue is further validated with ceramic CSP failure data.

Keywords: Solder joint fatigue, predictive modeling, design-for-reliability, flip-chip / chip-scale assemblies.

INTRODUCTION

Reliability Risks

Cyclic thermal stress conditions and mismatches in Coefficients of Thermal Expansion (CTEs) in surface mount assemblies lead to solder fatigue. Concerns have re-surfaced as advances in electronics packaging are placing more demand on solder interconnect reliability. Design characteristics that may impede FC and CSP assembly reliability include the following:

- CSPs are leadless and, with a few exceptions, their assemblies do not have much compliancy built-in. Compliancy helps relieve solder joint stresses as has been established with leaded packages having tall, compliant leads.
- Their effective CTEs tend to be low because of high silicon contents. Most existing CSPs are thus poorly CTE-matched to organic boards.
- Assembled packages have a low standoff height for miniaturization purposes. This increases cyclic shear strains in solder joints.
- FC and CSP micro-solder joints have smaller load bearing or crack propagation areas than conventional surface mount assemblies. Smaller load bearing areas imply higher solder joint stresses. Smaller crack propagation areas imply shorter crack propagation times. The two effects result in reduced fatigue lives.
- FC assemblies also suffer from competing, and often overwhelming, failure modes such as die cracking and underfill delamination.

Thermal Cycling Results

The above concerns are supported by accelerated thermal cycling test results [2-16] which suggest that, on a relative basis, most FC and CSP assemblies on organic boards are less reliable than their Plastic Ball Grid Array (PBGA) counterparts. For example, many PBGAs assembled on FR-4 have a median life of the order of 5,000-10,000+ cycles during thermal cycling between 0ºC and 100°C with typical dwell times of 5-10 minutes and at test frequencies in the range 24-72 cycles/day. Under similar conditions, existing CSP assemblies have median lives in the range 1,000-5,000 cycles, some as low as 5-100 cycles. To put those numbers in perspective, consider that a television set that is turned off and on an average of ten times a day will experience 36,500 thermal cycles, under milder conditions but with longer dwells, for an expected life of ten years.

Small Joint Effects

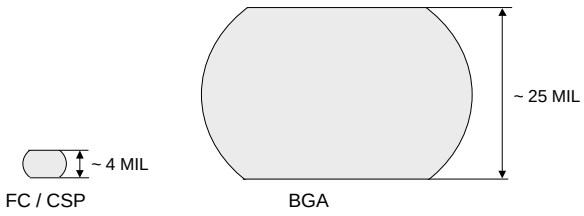

Figure 1: Relative size of FC/CSP and BGA joints. FC/CSP solder joints are two orders of magnitude smaller than BGA joints in volume.

The small joint size or volume effects are illustrated in Figure 1 with typical joint heights of the order of 3-4 mil for FC & CSP and 20-25 mils for BGAs:

† microBGA is a trademark of Tessera, Inc.

- For identical chips in a FC / CSP or BGA format, the joint height ratio of 25/4 = 6.25 implies FC / CSP solder joint shear strains perhaps 6.25 times higher than in BGA assemblies. Using a Coffin-Manson relationship [17] with a strain exponent of 2 for solder joint life estimates, the strain ratio could result in a fatigue life ratio of $6.25^2 = 39$, which is over one order of magnitude.
- With a volume ratio of about $(25/4)^3 = 244$, i.e. over two orders of magnitude, the energy absorbing capability of FC / CSP solder joints is significantly less than that of BGA solder joints.

While the reduced load bearing and crack propagation area of FC / CSP solder joints has a negative effect on fatigue lives, small solder joints may also have an improved fatigue resistance due to less flaws, less grain boundaries or less crack initiation sites than in larger joints. This is a well-known property of engineering metals whereby, under equal stress, smaller specimens have a longer life than larger ones [18]. This effect is demonstrated in a later section of this paper using FC and ceramic CSP solder joint failure data.

Clearly, the reliability of FC or CSP assemblies needs to be looked at carefully, more so than with conventional surface mount or area array assemblies. Solder joint modeling is an essential design tool for upfront reliability assessment and to extrapolate the results of accelerated test results to use conditions. The bulk of this paper focuses on the validation of the previously published Solder Reliability Solutions (SRS) model [1] for FC and CSP assemblies.

UNDERFILLED FLIP-CHIP RELIABILITY

Underfill Mechanical Requirements

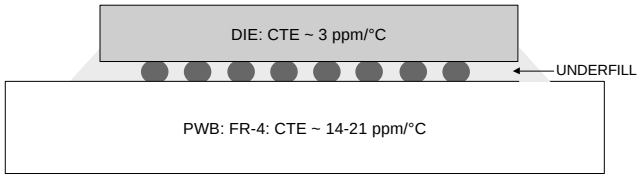

Figure 2: Schematic of underfilled flip-chip assembly.

The thermal expansion mismatch between the die and substrate in underfilled flip-chip assemblies (see schematic in Figure 2) is taken up by the solder joints AND the underfill layer, thus providing for solder joint strain relief. However, the mechanical coupling provided by the underfill layer stiffens the assembly. Die stresses increase and underfilled flip-chip assemblies are more sensitive to die cracking than bare die assemblies. Interfacial stresses between the underfill layer and the die or the substrate lead to a third potential failure mode, underfill delamination. Essential mechanical requirements for reliable flip-chip assemblies are summarized as follows:

- The modulus of the underfill material should be large enough to provide for effective coupling between the die and the substrate.
- The CTE of the underfill material should be close to that of solder to prevent stretching of the solder joints in the vertical direction.
- The die strength, which is very sensitive to surface defects, should be high enough to eliminate the risk of die cracking [12].
- The die / underfill and substrate / underfill adhesion strength should be high enough to eliminate delamination risks.

Underfilled Flip-Chip Model

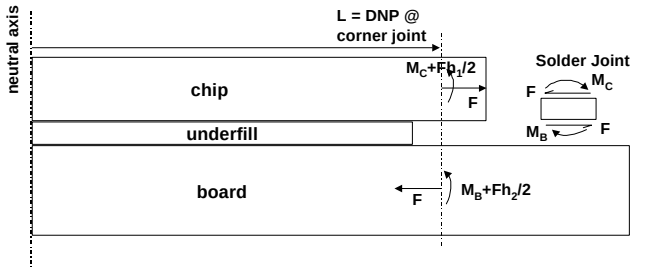

Figure 3: Schematic of half an underfilled assembly from the neutral axis to the outer most corner joint.

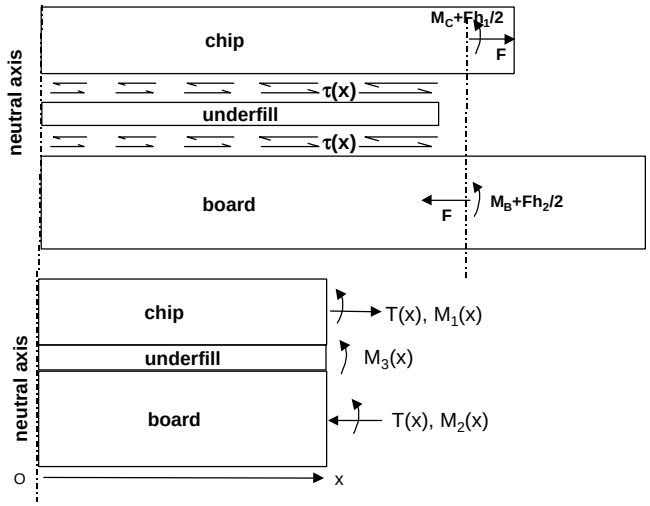

Figure 4: Interfacial shear stress distribution at die/underfill/substrate interfaces (top), and internal forces and moments in each layer of the assembly (bottom).

Figures 3 shows solder joint forces and moments at the outermost corner joint of an underfilled flip-chip assembly subject to a temperature swing. Figure 4 shows interfacial shear stresses along the underfill layer and the corresponding internal forces and moments in each layer of the assembly. The problem presented in Figures 3 and 4 was solved in a previous publication [19]. The strength of

materials solution provides stresses and strains everywhere in the assembly. Of most interest are the die stresses, the underfill shear stress distribution, and solder joint stresses and strains during thermal cycling. Details of the analytical procedure are given in [19] and need not be repeated here. More data has become available to validate the underfill model. The main results of the model validation process are presented in the rest of this section and are summarized as follows:

- Underfill shear strain predictions nicely fit shear strain distributions obtained by moiré interferometry.
- Interfacial stress indicators correlate well with underfill delamination results.
- Predicted die stress distributions are in good agreement with stress measurements obtained by stress sensors.
- FC solder joint reliability data from a dozen tests, with and without underfill, correlate well with a strain energy based fatigue life criterion.

Underfill Shear Strain Data

Figure 5 shows the good agreement between measured and predicted shear strains in the underfill layer of a silicon on ceramic assembly [20] subject to a temperature swing ΔT=-80ºC. Data points are shown as triangles. The predicted shear strain distribution is plotted for several values of the underfill Young's modulus, E_U.

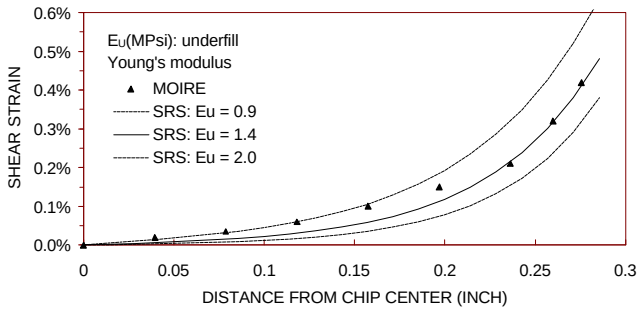

Figure 5: Shear strain distribution in underfill layer of silicon-on-ceramic test vehicle (ΔT = -80ºC).

In the high strain region towards the edge of the chip, the model fits best for E_U = 1.4 Mpsi. Sources of discrepancy between measured and predicted strains include simplifications inherent to the strength of materials approach, uncertainties in material properties, the possible temperature dependence of underfill properties, and the absence of end fillet effects in the model.

Interfacial Shear Stresses

The underfill model was applied to thermal cycling experiments conducted at Motorola [21, 22]. Test vehicles were from three different vendors, A, B and C. Underfill delamination was the primary failure mode during air cycling and Liquid-to-Liquid Thermal Shock (LLTS) from -55 to 125ºC. Vendor differentiating parameters were the board CTE, Young's modulus and the underfill layer thickness.

Figure 6 shows the correlation of maximum shear stresses at the end of the underfill layer versus cycles-to-failure for the three assembly types and two test conditions. The difference between air cycling and LTTS is attributed to the statistical nature of cycles-to-failure, with the LTTS data being averaged over several lots and the air cycling data being from a single lot, as well as differences in dwell times (5 minutes for LTTS, 20 minutes for air-to-air).

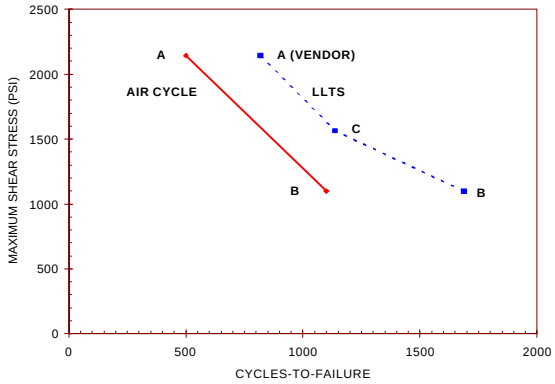

Figure 6: Maximum shear stress in underfill layers versus cycles-to-failure from Motorola's experiments [21, 22].

The trendlines in Figure 6 cannot be used directly for predictive modeling since the model does not capture the detailed dynamics of delamination failures. However, since solder joint failures occur in a short period of time after underfill delamination begins, the calculated maximum shear stress can serve as an indicator of delamination risk in comparative studies looking at changes in design parameters and/or material properties.

Die Stress Data

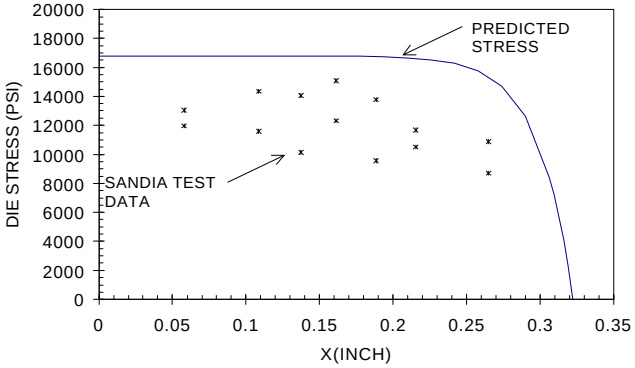

Figure 7: Predicted and measured die stresses in Sandia's test vehicle (data after [23, 24]).

Figure 7 shows profiles of predicted and measured compressive die stresses on the flip-chip side of Sandia's test die [23, 24] after cooling of the underfilled assembly from 160°C to 20°C. The stress profile is along the chip diagonal from the center to a corner of the die. Stress measurements were obtained on a test chip with built-in stress sensors. Given the scatter of the data, predicted stresses are in good agreement with stress measurements. Predictions are slightly higher, i.e. on the conservative side, possibly because of uncertainties in material properties and because the underfilled flip-chip model does not account for the lower modulus of the underfill material at elevated temperatures.

The predicted stresses drop to zero the furthest away from the center of the die because of the stress-free boundary condition at the edge of the die. The maximum die stress is at the center of the die. However, the stress profile is rather flat over a large portion of the die. This implies that die integrity will be sensitive to surface defects or handling scratches over most of the die area.

Correlation of Solder Joint Fatigue Data

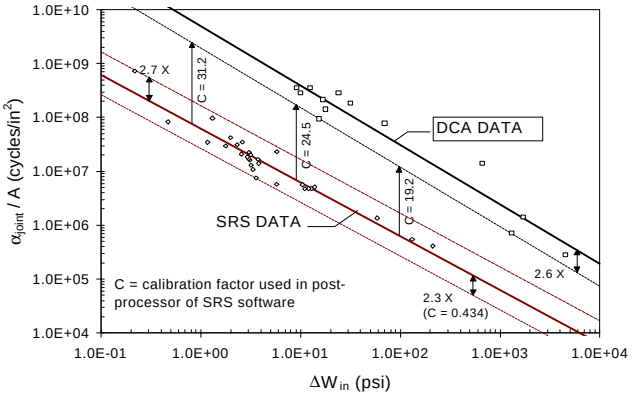

Figure 8: Correlation of solder joint failure data for conventional SMT (shown as diamonds) and underfilled DCA assemblies (shown as squares). Cycles-to-failure scaled for the solder crack area are plotted versus cyclic inelastic strain energy.

Figure 8 first shows the original correlation of SRS solder joint failure data, i.e., characteristic life (on a per joint basis) scaled for the solder crack area versus cyclic inelastic strain energy. The reader is referred to [1] for background information on the SRS model. The correlation of SRS data (shown as diamonds) is for conventional SMT test vehicles including leadless and leaded assemblies and PBGA test vehicles. The least-square goodness of fit correlation coefficient of the conventional SMT data is 0.965. The equation of the centerline correlation (i.e. the "SRS data" solid line in Figure 8) is:

$$\frac{\alpha_{JOINT}}{A} = \frac{6.149\times10^{7}\times C}{\Delta W^{0.998}} \qquad (1)$$

where:

- α_{JOINT} (cycles) is the characteristic life or cycles to 63.2% failures in the joint population.
- A (in^2) is the solder crack area for fully cracked electrically open solder joints (also the minimum solder joint load bearing area).
- ΔW ($lb.in/in^3$ or psi) is the cyclic inelastic strain energy per unit volume obtained as the sum of strain energies due to global and local CTE mismatches.
- C is a model calibration factor:
  - ◊ C = 1 for the center line (solid line of SRS data correlation band),
  - ◊ C = 0.434 for the lower bound of the test data (a factor 2.3 X below the centerline),
  - ◊ C = 2.7 for the upper bound of the correlation (a factor of 2.7 X above the centerline).

Figure 8 also shows that a similar correlation holds for Direct Chip Attach (DCA) or underfilled flip-chip solder joints. The DCA failure data, shown as rectangles, is from [25]. The 13 data points include thermal cycling results for assemblies with and without underfill, different solder joint heights, several underfill and substrate materials. The equation of the DCA centerline correlation ("DCA data" solid line at the top of Figure 8) is:

$$\frac{\alpha_{JOINT}}{A} = \frac{5\times10^{9}}{\Delta W^{11032}} \qquad (2)$$

The least-square goodness-of-fit correlation coefficient for the 13 DCA data points is 0.967. The DCA dataset has a lower bound a factor 2.6 X below the solid centerline.

The centerline correlations for conventional SMT and for DCA assemblies both have slopes close to -1, which is consistent with existing strain energy based models for SMT assembly reliability [1, 26-30]. However, the DCA data is offset upwards by a large factor, as shown in Figure 8. The offset of the DCA data possibly relates to the much smaller size of DCA solder joints, a well-known effect in mechanics and fatigue of materials. The DCA joints, which are much smaller than conventional SMT or BGA solder joints, contain relatively few grains and thus have less “flaws” or weak sites for grain boundary sliding and/or crack growth. In mechanical or fatigue testing of engineering materials, small volume specimens have higher strength or improved fatigue life over larger specimens [18] because of the smaller number of flaws or crack initiation sites in a smaller volume of material.

The scaling of flip-chip fatigue lives for the solder crack area thus needs to be adjusted for the phenomena discussed above. In the next section, we will show that a volume correction factor can be used to bring together the SMT and DCA datasets in Figure 8. Alternatively, users of the SRS model have used the calibration factors (coefficient "C" in

equation (1)) given by equation (3) below to estimate the reliability of underfilled flip-chip assemblies.

The offset between the DCA and SRS correlation lines is not quite constant because of slight differences in slopes. From equations (1) and (2), the calibration factor to go from the centerline of the SRS data to the lower bound of the DCA correlation band is:

$$C = \frac{3127}{\Delta W^{0.1052}} \qquad (3)$$

The plot of DCA test data in Figure 8 gives values of C = 19.2, 24.5 and 31.2 for strain energies of 100 psi, 10 psi and 1 psi, respectively. The lower bound of the DCA data is a factor 2.6 X below the DCA centerline ("DCA data" solid line in Figure 8). To predict life based on the DCA centerline, multiply the calibration factor in equation (3) by 2.6.

IMPACT OF SOLDER VOLUME ON SOLDER JOINT FATIGUE

Fatigue Data Correlation

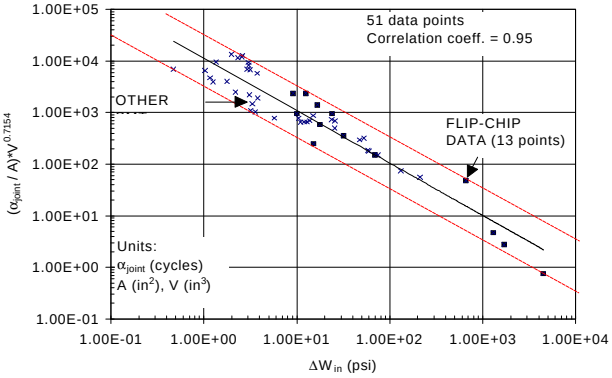

Figure 9: Correlation of conventional SMT and flip-chip failure data. Horizontal axis is the cyclic inelastic strain energy. Vertical axis is cycles-to-failure, scaled for the solder crack area, times a volume correction factor.

The failure data for conventional SMT and flip-chip solder joints in Figure 8 are brought together in Figure 9 by means of a solder volume correction factor. That is, the correlation shown in Figure 9 is similar to the original correlation of the SRS model, with an added volume correction factor on the vertical axis. The correlation is based on 51 datasets, 38 of which are for conventional SMT plus the 13 flip-chip datasets from [25]. The equation of the centerline correlation in Figure 9 is:

$$\frac{\alpha_{JOINT}}{A} \times V^{0.7154} = \frac{11329}{\Delta W^{1.016}} \qquad (4)$$

where the solder joint volume V has units of inch^3. The goodness-of-fit correlation coefficient for the 51 data points in Figure 9 is 0.95. Spread of the data around the centerline is a factor of two to three times, which is typical of fatigue data correlations.

Discussion

The introduction of a volume correction factor is more than a simple curve fitting operation and is motivated by the sizable effect of specimen volume on the fatigue life of engineering metals. The 51 datasets in Figure 9 cover a wide range of solder volume, including solder joints of conventional LCCCs, SOTs, fine-pitch QFPs, TSOPs, BGAs and underfilled flip-chip assemblies. That is, the correlation is based on a variety of component types and evolving technologies. In addition, as in previous correlations of solder joint fatigue data [1, 26-30], equation (4) has a strain energy exponent that is close to -1.

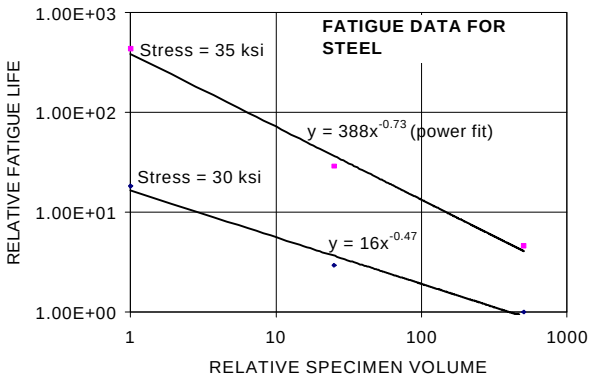

Figure 10: Correlation of fatigue life versus volume of steel specimens tested at two stress levels (data after [18]). Power curve fitting gives volume exponents of -0.73 and -0.47.

Last, the volume exponent in equation (4) is in the range of exponents -0.73 to -0.47 given in Figure 10 for the correlation of fatigue data versus specimen volume for a steel alloy tested at two stress levels.

Model Calibration Factors

For users of the original SRS model to use the new correlation with volume correction effects, the model calibration factor C is obtained from equations (1) and (4):

$$\frac{6.149 \times 10^{7} \times C}{\Delta W^{0.998}} = \frac{11329}{\Delta W^{1.016}} \times \frac{1}{V^{0.7154}} \qquad (5)$$

After dropping the strain energy terms, which have similar exponents, we get:

$$C \approx \frac{1.8424 \times 10^{-4}}{V^{0.7154}} \qquad (6)$$

where the solder volume has units of inch^3. Using a model calibration factor given by equation (6) in the SRS post-processor [31] gives life predictions based on the centerline correlation in Figure 9.

MICRO-BGA RELIABILITY

Package Construction

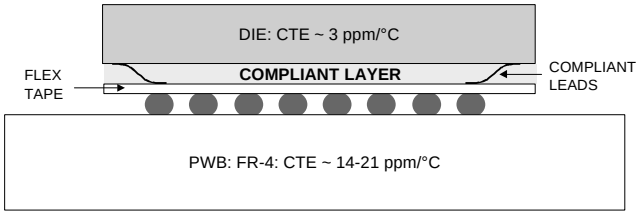

Figure 11: Schematic of micro-BGA on a circuit board.

Figure 11 is a schematic of a micro-BGA package mounted on a circuit board. The package most distinctive feature is a low modulus compliant elastomer layer that provides for decoupling between the silicon die and the flex tape at the bottom of the package [32-34]. During thermal cycling, the compliant elastomer layer, with Young's modulus of a few hundred psi, is essentially in shear. Shear is driven by the CTE mismatch between the die and the flex tape as well as external forces and moments that the solder joints exert on the package. With an elastomer layer that is compliant enough, the solder joints will only see the CTE mismatch between the flex tape and the circuit board.

Micro-BGA Model

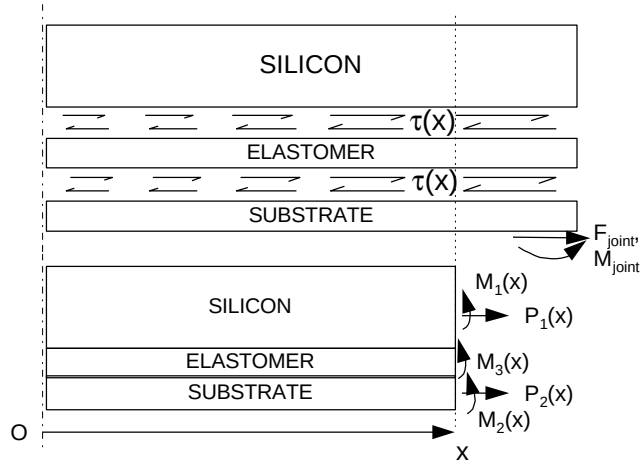

Figure 12: Internal stresses in micro-BGA package. Only half of the package is shown, from the neutral axis to an outermost corner joint.

Figure 12 shows the assumed shear stress distribution, $\tau(x)$, in the elastomer layer, forces and moments exerted by the solder joints (F_{joint}, M_{joint}) and internal forces and moments ($P_i(x)$, $M_i(x)$) in a vertical cross-section of the package. Stresses and strains in the micro-BGA package are solved for by using existing theories of multilayer stacks and adhesive bonds, similar to the solution that was discussed before for underfilled flip-chip assemblies. The effective package CTE that is seen by the solder joints is derived from calculated strains on the bottom side of the package. For assembly stiffness calculations, the stretching and bending stiffness of the package are obtained as functions of chip size, geometry and material properties of the different layers of the package.

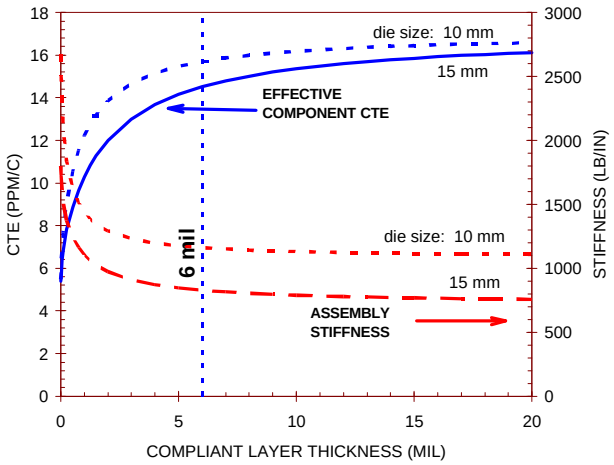

Figure 13: Micro-BGA effective CTE and assembly stiffness as a function of elastomer layer thickness.

The micro-BGA model was applied to a generic micro-BGA mounted on a 0.062" FR-4 board and with a 15 mil thick die. Material properties that were used are from [34]. Figure 13 shows the effective package CTE and assembly stiffness as a function of thickness of the compliant elastomer layer. The effective package CTE increases and the assembly stiffness decreases as the elastomer thickness increases. The elastomer layer has to be thick enough to provide an effective package CTE that is close to the CTE of FR-4 boards. For a thickness of 6 mil, the effective CTE is in the range 15.7 ppm/ºC (10 mm die) to 14.5 ppm/°C (15 mm die). Beyond 6 mils, incremental gains in effective CTE and assembly compliance are limited. Nevertheless, with a minimum thickness of the compliant elastomer, the package-to-board CTE mismatch and the assembly stiffness are greatly reduced when compared to the situation of bare chips on FR-4.

Results of the above parametric study are in agreement with the conclusions of finite element studies in [34] and suggest that the micro-BGA model quantify the chip-to-flex decoupling well. Further validation of the micro-BGA model is presented below using thermal cycling test results.

Validation of Micro-BGA Reliability Model

Thermal cycling solder joint failure data were published recently [4, 5] for 144 I/O micro-BGAs assembled on printed wiring boards. Thermal cycling conditions were from 0ºC to 100ºC with 15 minute dwells at the temperature extremes and a test frequency of 36 cycles/day. Typical characteristic lives for several board pad diameters (10, 14 and 16 mil) and standoff heights (13-16 mil) were in the range 1000-2000 cycles. Several board finishes were

used, some resulting in infant mortality failures. Boards with imidazole Organic Solderability Preservative (OSP) were not prone to infant mortality failures and gave nice failure distributions. We used solder joint characteristic lives from the OSP test boards to assess the applicability of the SRS model to micro-BGA assemblies.

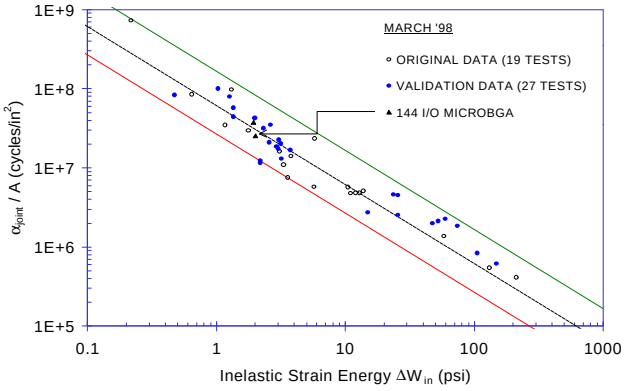

Figure 14: Fit of micro-BGA solder joint failure data to the correlation band of the SRS model. The micro-BGA data points are shown as dark solid triangles.

The results are shown in Figure 14 where the micro-BGA failure data (shown as dark solid triangles) fall within the original correlation band of the SRS model. The micro-BGA data are actually very close to the model centerline. Other data points in Figure 14 include the 19 original tests that were used to establish and freeze the correlation band, plus 27 validation points including PBGA, CBGA, TSOP and QFP reliability data. Model validation is an on-going process. We plan to further validate the use of the SRS model for micro-BGA assemblies when additional test results become available, including solder joint failure distributions and test vehicle design parameters.

CERAMIC CSP RELIABILITY

Test Vehicles

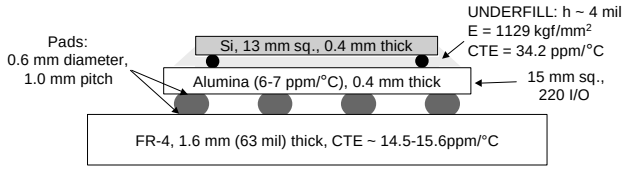

Figure 15: Schematic of 220 I/O ceramic CSP mounted on FR-4 board. Test vehicle parameters are from [6,35].

The ceramic CSP is a package with an alumina interposer. The package can be thought of as a shrunken Ceramic Ball Grid Array (CBGA). Figure 15 is a schematic of a ceramic CSP with design parameters from test vehicles described in [6, 35]. Packages of two sizes: 116 I/Os (11 mm square) and 220 I/Os (15 mm square) were assembled on FR-4 using eutectic paste or solder balls and paste. Test conditions were thermal cycling between -40ºC and 125°C with 20 minute dwells at the temperature extremes and a test frequency of 24 cycles/day. For the 220 I/O CSPs assembled with paste only, first failures occurred at about 500 cycles. For the 220 I/O CSP assemblies with solder balls, and thus a higher standoff height, first failures occurred at about 900 cycles. Readers are referred to [6, 35] for more detailed information on the test vehicle design parameters and the results of the ceramic CSP design-of-experiments.

Ceramic CSP Model

The ceramic CSP substrate is 0.4 mm thick. Accelerated test results suggest that CBGA assemblies with 1 mm thick substrates have a fatigue life 2.5 times longer than CBGA assemblies with a 2.9 mm thick substrate [36]. This life improvement is attributed to the greater flexibility of the thin CBGA substrate. Similarly, the ceramic CSP with an even thinner (0.4 mm) substrate is expected to flex during thermal cycling. That is, the thin alumina substrate provides compliancy to the assembly.

Thus, for mechanical modeling purposes, the ceramic CSP is treated as a multilayer structure with three layers of alumina, underfill and silicon that can stretch and bend. Using an existing multi-layer model that was developed and validated for PBGAs [1, 37], we can estimate the effective CTE at the bottom of the ceramic CSP, as well as the stretching and bending stiffness of the package. The above parameters are important parameters of the SRS model. Readers are referred to [1, 37] for details on the PBGA multi-layer model. The package effective CTE and the package spring constants are estimated in the model based on the specific input of thickness, elastic properties (Young's modulus and Poisson's ratio) and CTEs of each layer in the ceramic CSP structure.

Validation of Ceramic CSP Reliability Model

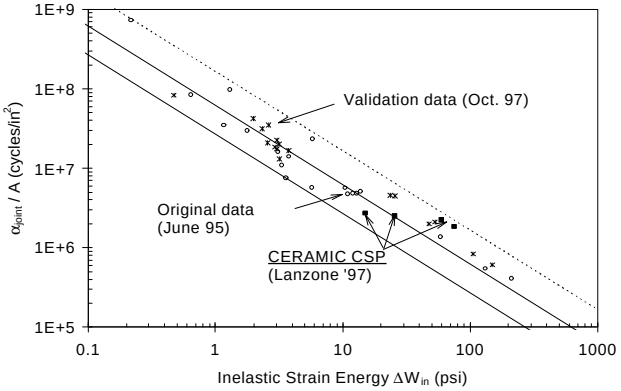

Figure 16: Fit of 116 and 220 I/O ceramic CSP board level failures to the original SRS model correlation band (CSP data after [6, 35]).

Test results are plotted on the original SRS correlation band in Figure 16. The ceramic CSP data are shown as

dark solid triangles, one for a 116 I/O CSP assembly with a stand-off height of 0.12 mm (4.7 mil) and the other three for 220 I/O CSP assemblies with different stand-off heights: 0.12 mm (4.7mil), 0.35 mm (13.7 mil) and 0.55 mm (21.6 mil). The four data points fall within the model correlation band. However, an even better fit is achieved when adding-in the solder volume correction factor, as shown below.

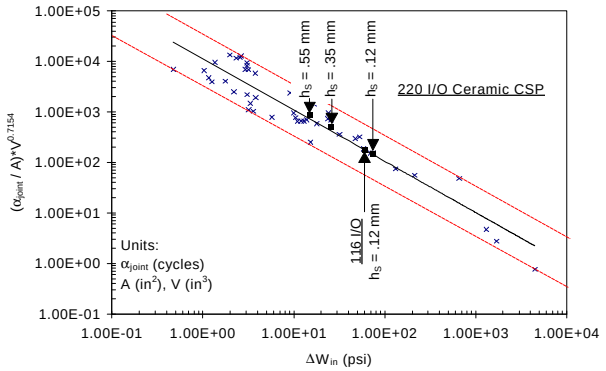

Figure 17: Fit of 116 and 220 I/O ceramic CSP board level failures to the SRS correlation band with volume correction factor on the vertical axis.

The same ceramic CSP test results are plotted in Figure 17 which includes the solder volume correction factor on the vertical axis of the SRS correlation of test data. The ceramic CSP data points fall very close to, and line up almost parallel to the model centerline. The better fit of the data for ceramic CSPs with different solder joint sizes is further evidence of the solder volume effect.

CONCLUSIONS

Findings of this study are summarized as follows:

- Establishing the reliability of FC and CSP assemblies for user specific conditions has become more critical than for previous SMT technologies. Available test results for existing CSPs are not as good as for PBGA assemblies.
- The SRS solder joint reliability model has been validated for flip-chip assemblies, micro-BGAs and CSPs with an alumina interposer.
- The existing SRS correlation of solder joint fatigue lives has been refined to include a solder volume correction factor.
- The solder volume correction factor captures the well-known effect of specimen size, i.e. the solder joint volume, on the fatigue life of metals.
- Related engineering mechanics models accurately predict die stresses and underfill strains in flip-chip assemblies.
- The above improvements in the SRS approach, and the extension of the model to flip-chip and CSP assemblies, can be of help to qualify emerging assembly technologies in the early stages of product development. The models provide the most value in upfront reliability assessment projects -- the preferred approach of reliability conscious organizations.
- The models are also of use to derive acceleration factors and to extrapolate test failure distributions to field use conditions.

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