SMT / CSP RELIABILITY PERSPECTIVES

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Cyclic thermal stress conditions lead to solder joint creep-fatigue, a possible cause of failure in SMT assemblies. Lessons learned since the inception of SMT can provide guidelines for establishing the reliability of emerging Chip Scale Package (CSP) assemblies.

LESSONS LEARNED

Design factors that affect attachment reliability include global mismatch between in-plane Coefficients of Thermal Expansion (CTEs) of components and boards, the assembly or lead stiffness, and local CTE mismatches between solder (CTE ~ 24 ppm/°C) and the interconnected parts. Accelerated Thermal Cycling (ATC) results in Table 1 show reliability trends and attest to the importance of these effects for components mounted on FR-4.

COMPONENT	MEAN CYCLES TO FAILURE	GLOBAL CTE MISMATCH	LOCAL CTE MISMATCH (relative importance)	ASSEMBLY STIFFNESS (LB/IN)
68 I/O LCCC	< 100	HIGH	LOW	2000-10000
68 I/O PLCC	> 10,000	LOW	LOW	~ 50
132-256 I/O PQFP (with copper leads)	> 10,000	LOW	LOW	~ 10-20
32 I/O Alloy42 TSOP	500-1000	HIGH	HIGH	150-300
225 I/O PBGA	3000-12,000	LOW-MEDIAN	LOW-MEDIAN	~ 5000

Table 1: Impact of CTE mismatches and assembly stiffness on solder joint fatigue life under ATC conditions (0 to 100°C, 5 to 30 minutes dwells).

- LCCC assemblies may fail rapidly due to the large CTE mismatch between ceramic and FR-4.
- PLCC and PQFP assemblies survive much longer thanks to tall, *compliant leads*.
- Alloy 42 TSOPs may not fare as well for three reasons: 1) the in-plane CTE of the package is low (6-10 ppm/°C) because of its high silicon content; 2) the lead stiffness is higher than for PQFPs because of the low-profile of the package; 3) Alloy 42 leads (CTE ~ 5 ppm/°C) have a large local mismatch with solder.
- The reliability of plastic BGAs (PBGAs) solder joints varies with parameters such as die size, laminate thickness, pad design, molding compound properties and stand-off height.

The main lessons learned are: **"Minimize CTE Mismatches" and "Build-In Compliance".**

CSP ASSEMBLIES

Much more so than with conventional SMT, the reliability of emerging CSP assemblies is application-dependent, cannot be taken for granted and needs to be evaluated on a case-by-case basis. Upfront reliability assessment, including careful characterization of materials, accelerated testing and modeling are key to the deployment of reliable CSP products.

Lead-On-Chip (LOC) packages have short and stiff leads, possibly a reliability-limiting factor. Most other CSPs are leadless and have a relatively large silicon content (CTE ~ 3 ppm/°C). Since expansion mismatch between components and substrates can be large, increasing chip and package sizes may be pushing the assembly reliability envelope. Reliability risks are minimized when strain-reduction mechanisms are built-in, i.e. in underfilled flip-chip and μBGA assemblies. On the other hand, CSPs such as Small Outline No-lead (SON) packages have an internal structure reminiscent of TSOPs but without external leads to alleviate solder joint reliability concerns. Establishing their attachment integrity requires careful consideration of all parameters involved, from material properties and geometry to expected use conditions and target design life.